20E220 6th2801

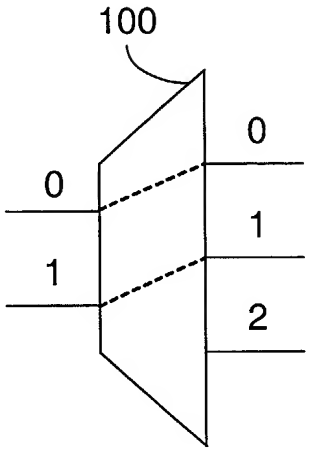

FIG. 1A

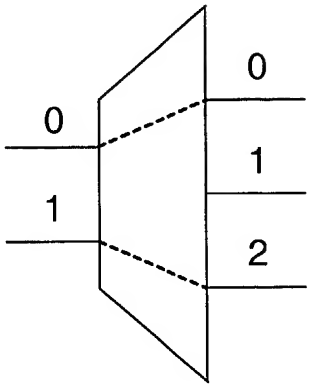

FIG. 1B

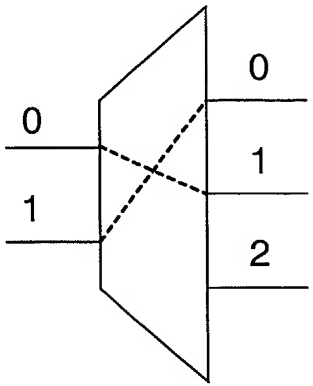

FIG. 1C

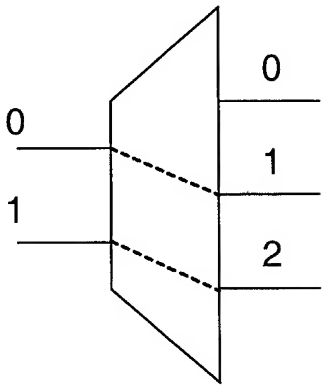

FIG. 1D

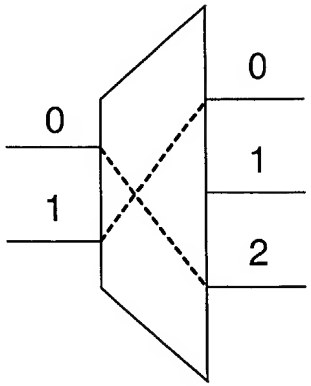

FIG. 1E

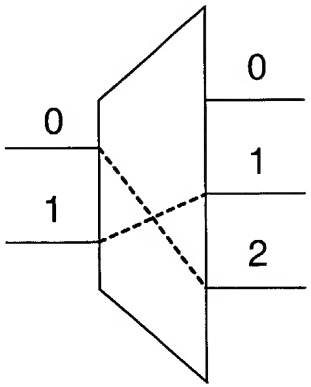

FIG. 1F

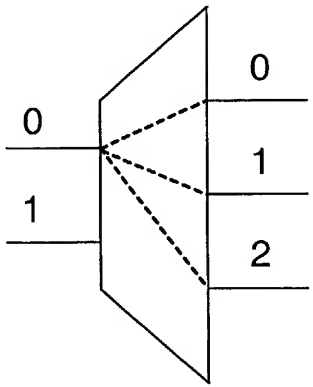

FIG. 1G

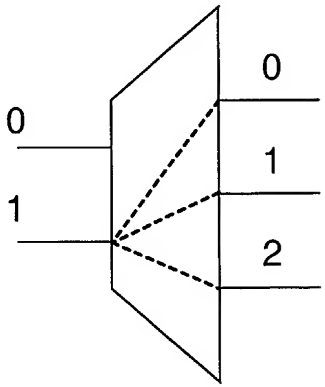

FIG. 1H

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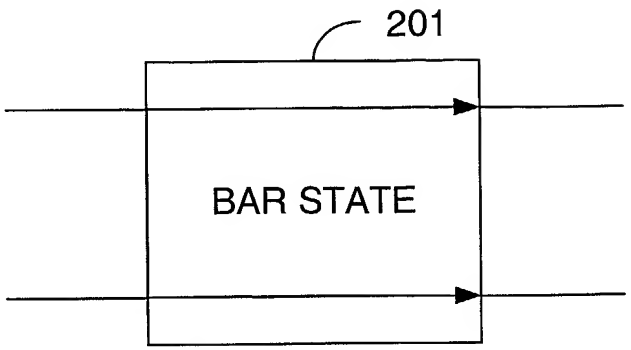


FIG. 2A

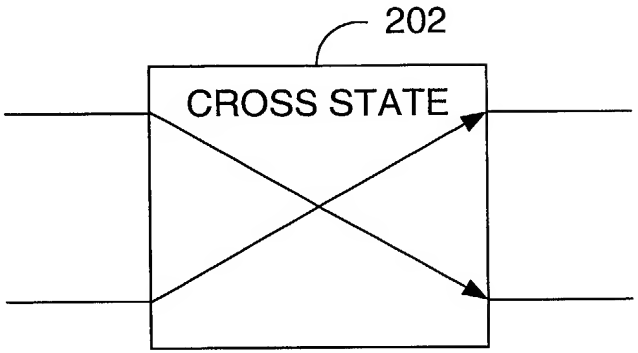


FIG. 2B

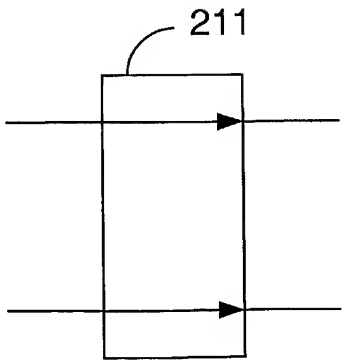


FIG. 2C

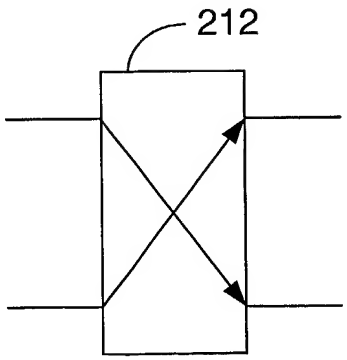


FIG. 2D

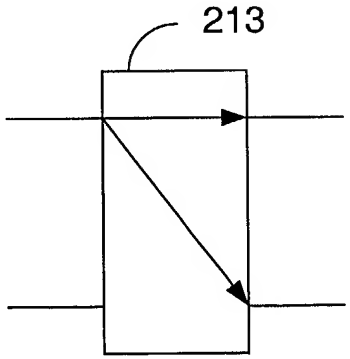


FIG. 2E

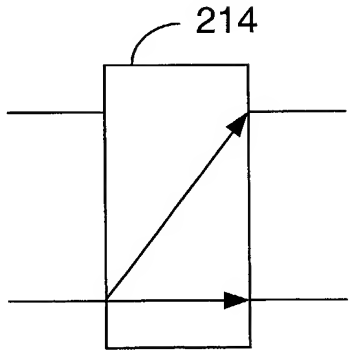


FIG. 2F

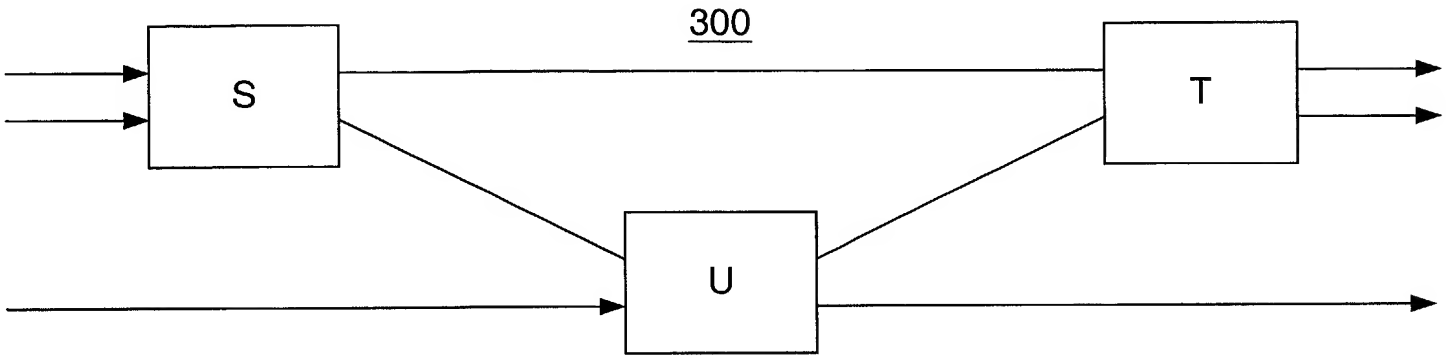


FIG. 3A

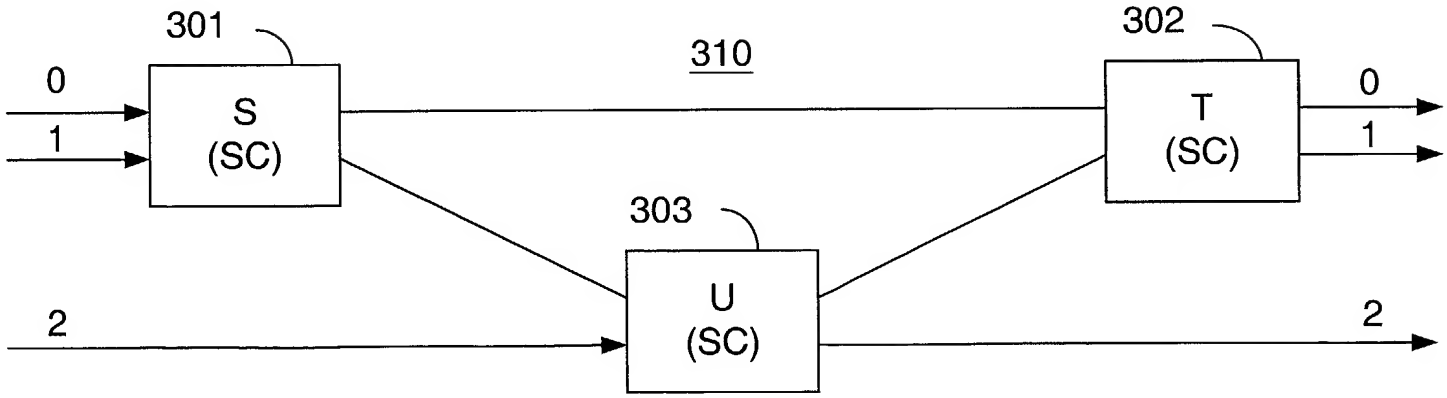


FIG. 3B

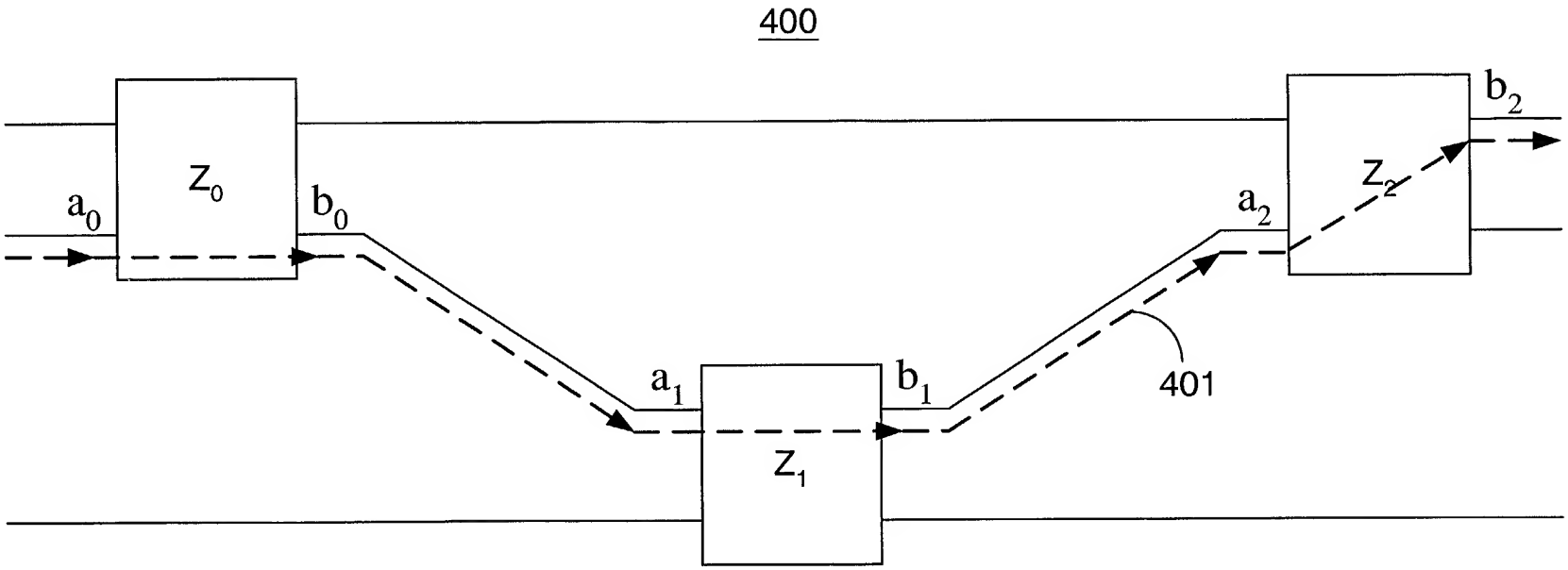


FIG. 4

Sheet 5 of 9 - 09/26/2005

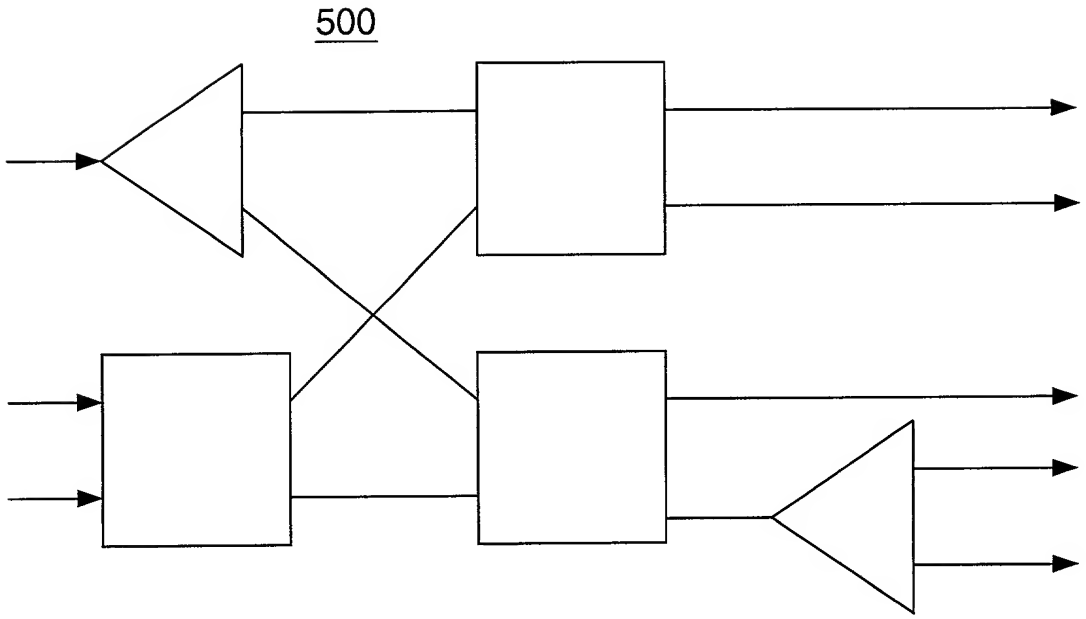


FIG. 5A

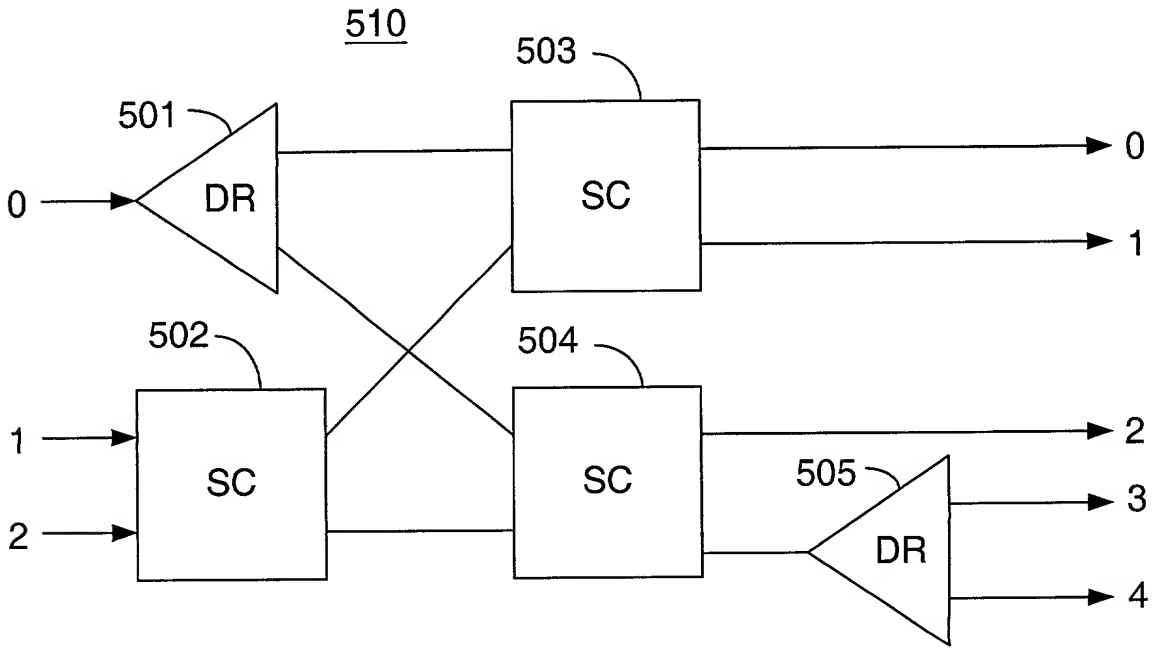
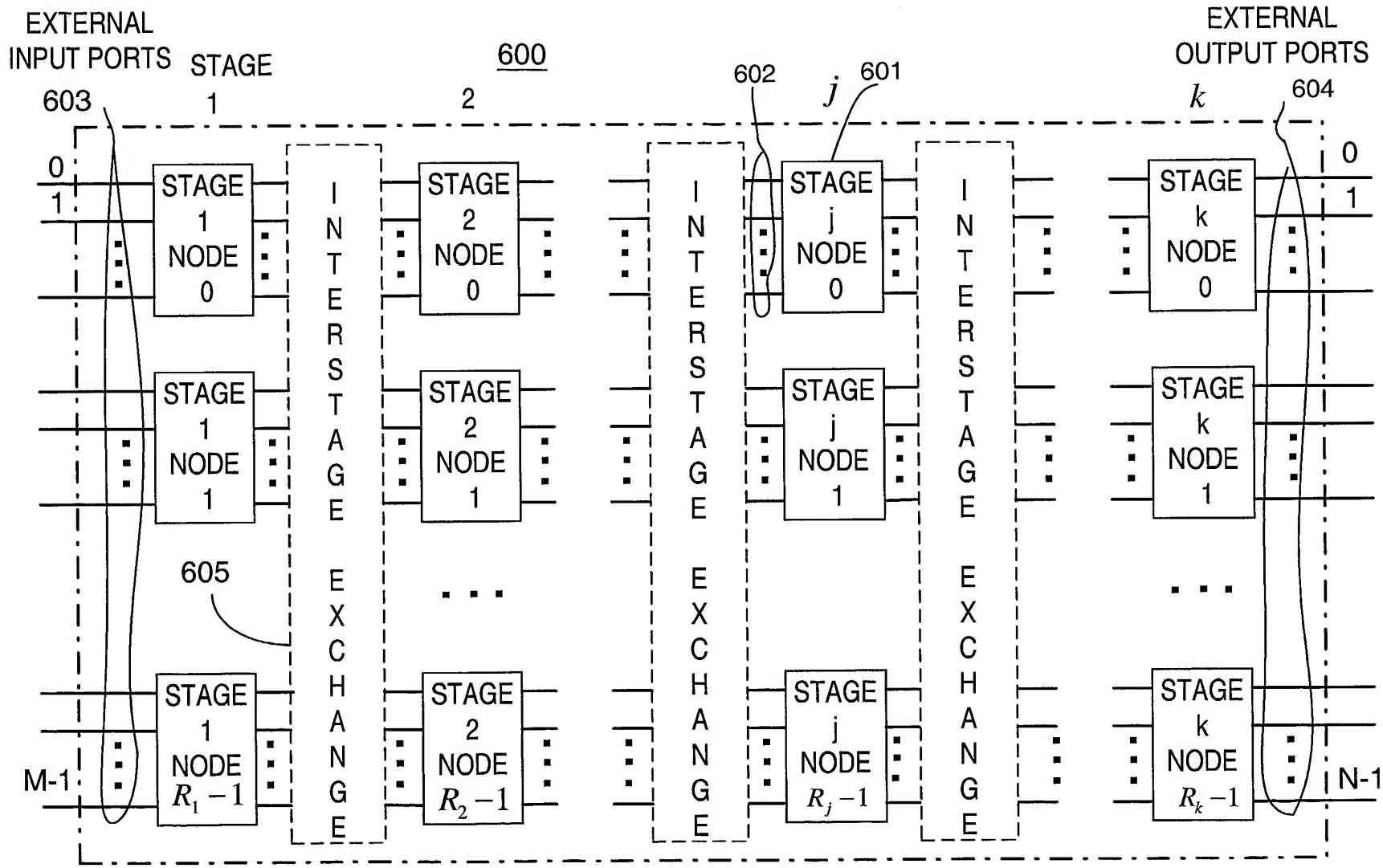


FIG. 5B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603
STAGE
1
600
2
602
j
601
k
604
EXTERNAL
OUTPUT PORTS
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1
M-1
STAGE 1 NODE 0
STAGE 1 NODE 1
STAGE 1 NODE $R_1 - 1$
INTERSTAGE EXCHANGE
STAGE 2 NODE 0
STAGE 2 NODE 1
STAGE 2 NODE $R_2 - 1$
INTERSTAGE EXCHANGE
STAGE j NODE 0
STAGE j NODE 1
STAGE j NODE $R_j - 1$
INTERSTAGE EXCHANGE
STAGE k NODE 0
STAGE k NODE 1
STAGE k NODE $R_k - 1$
605
N-1

FIG. 6A

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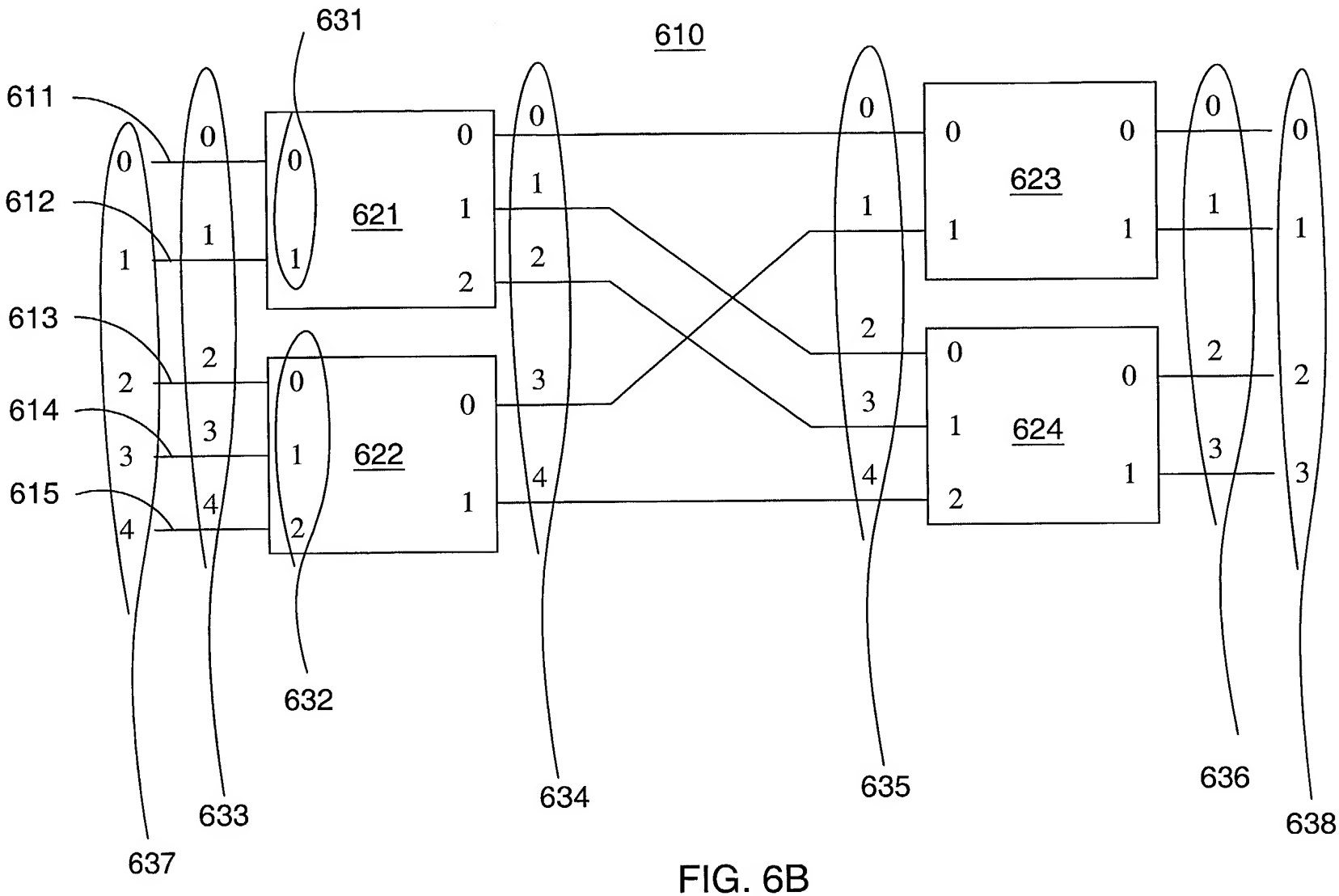

FIG. 6B

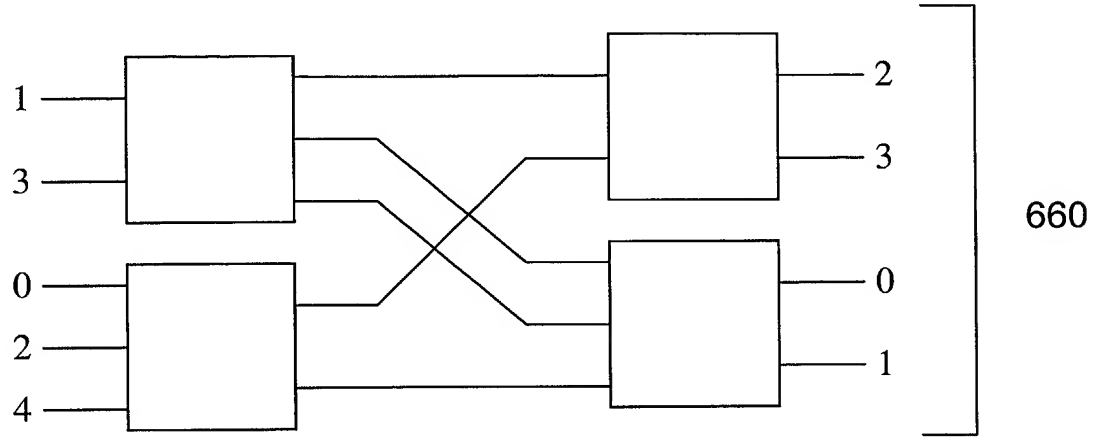
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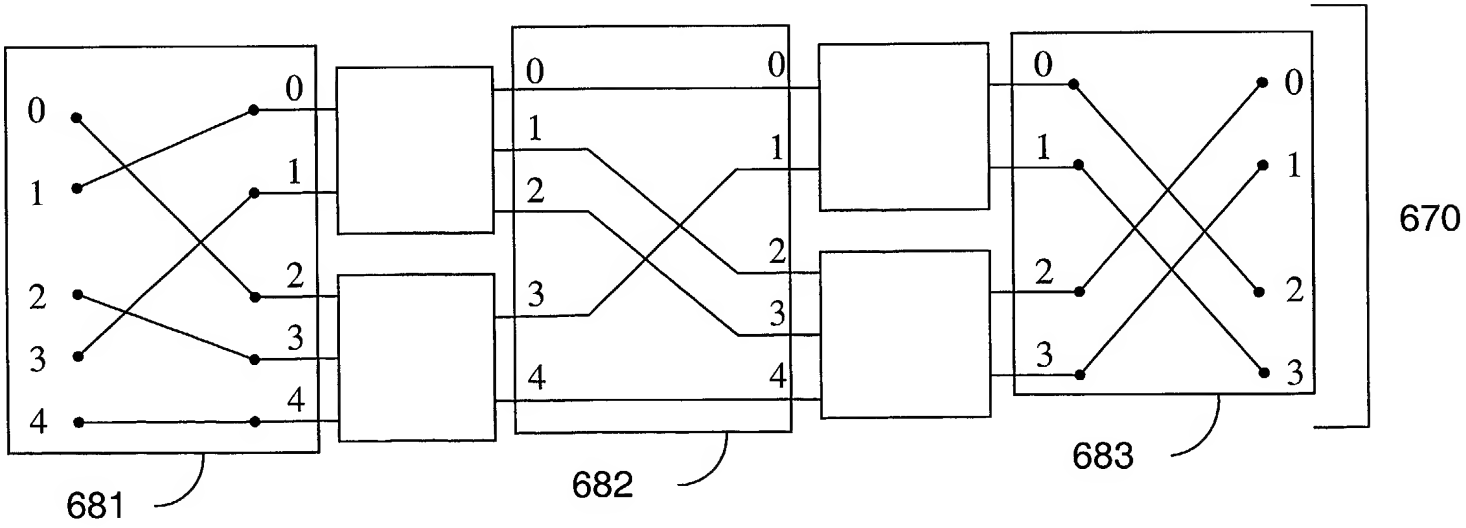
FIG. 6C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682
0
1
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3
0
1
2
3
683
670

FIG. 6D

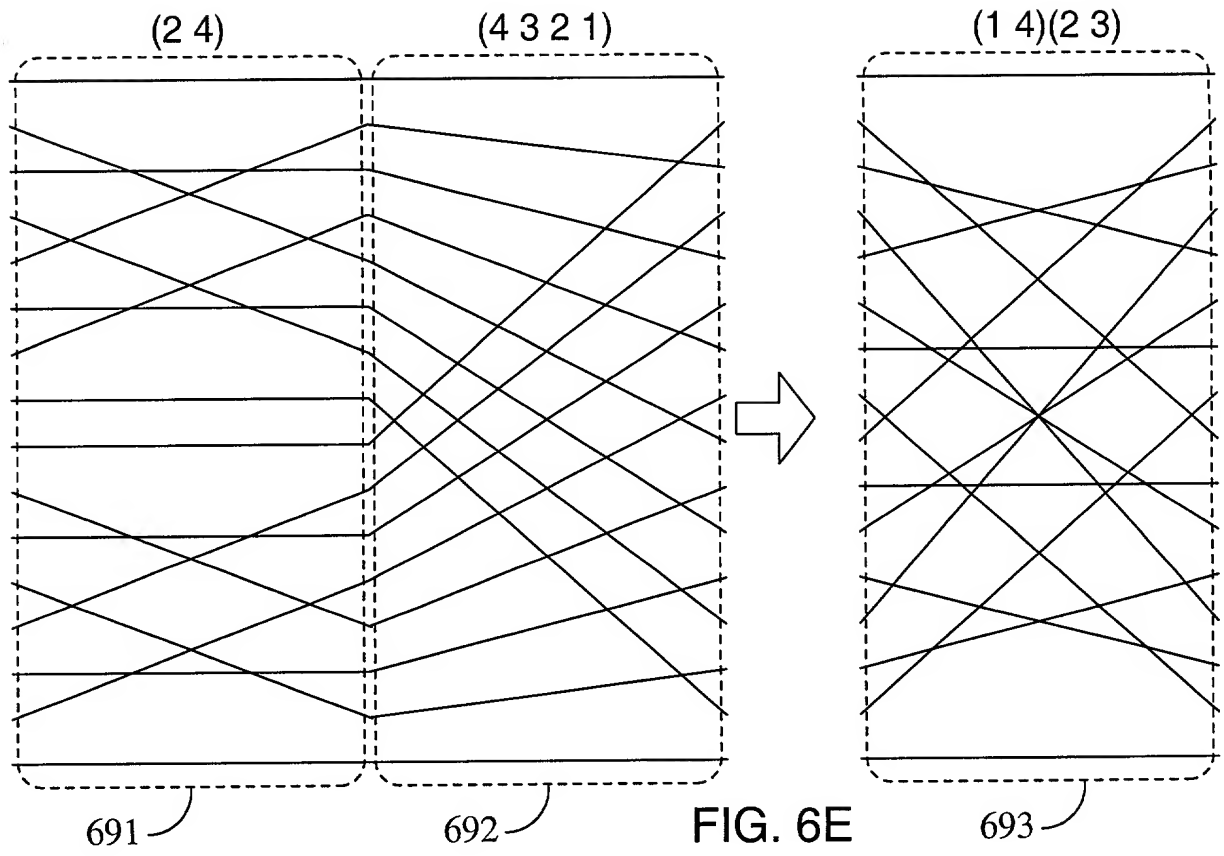

FIG. 6E

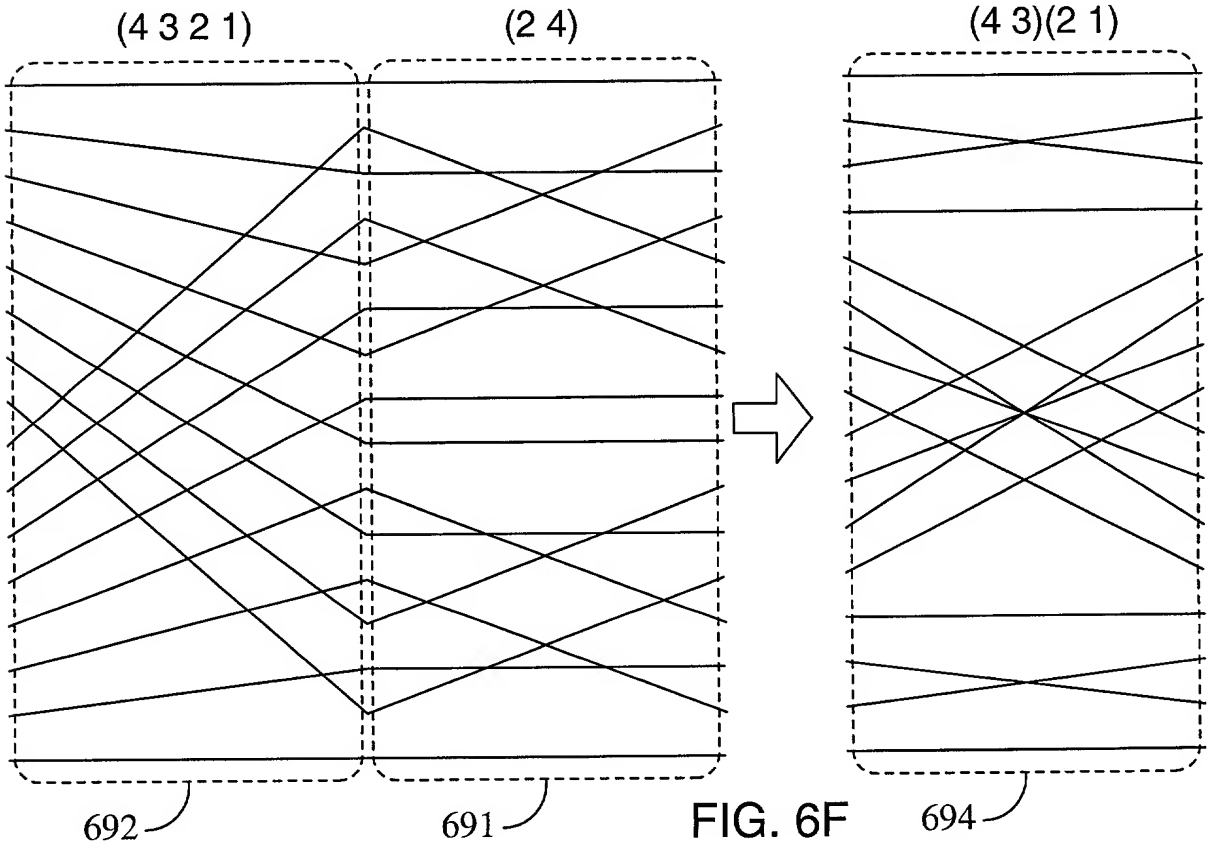

FIG. 6F

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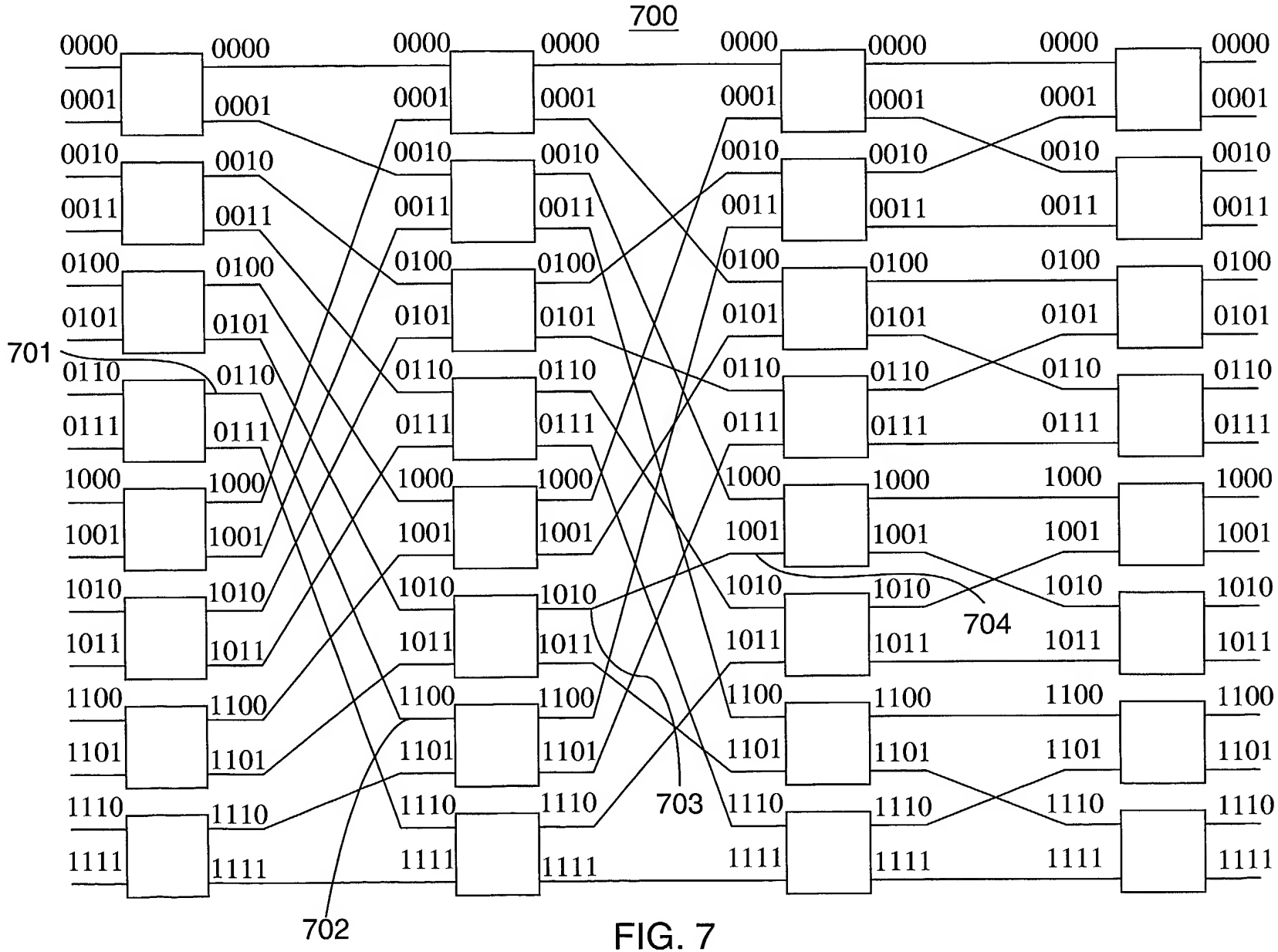
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0101
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0111
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1010
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1110
1111
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FIG. 7

Docket No. 0000.0000

800

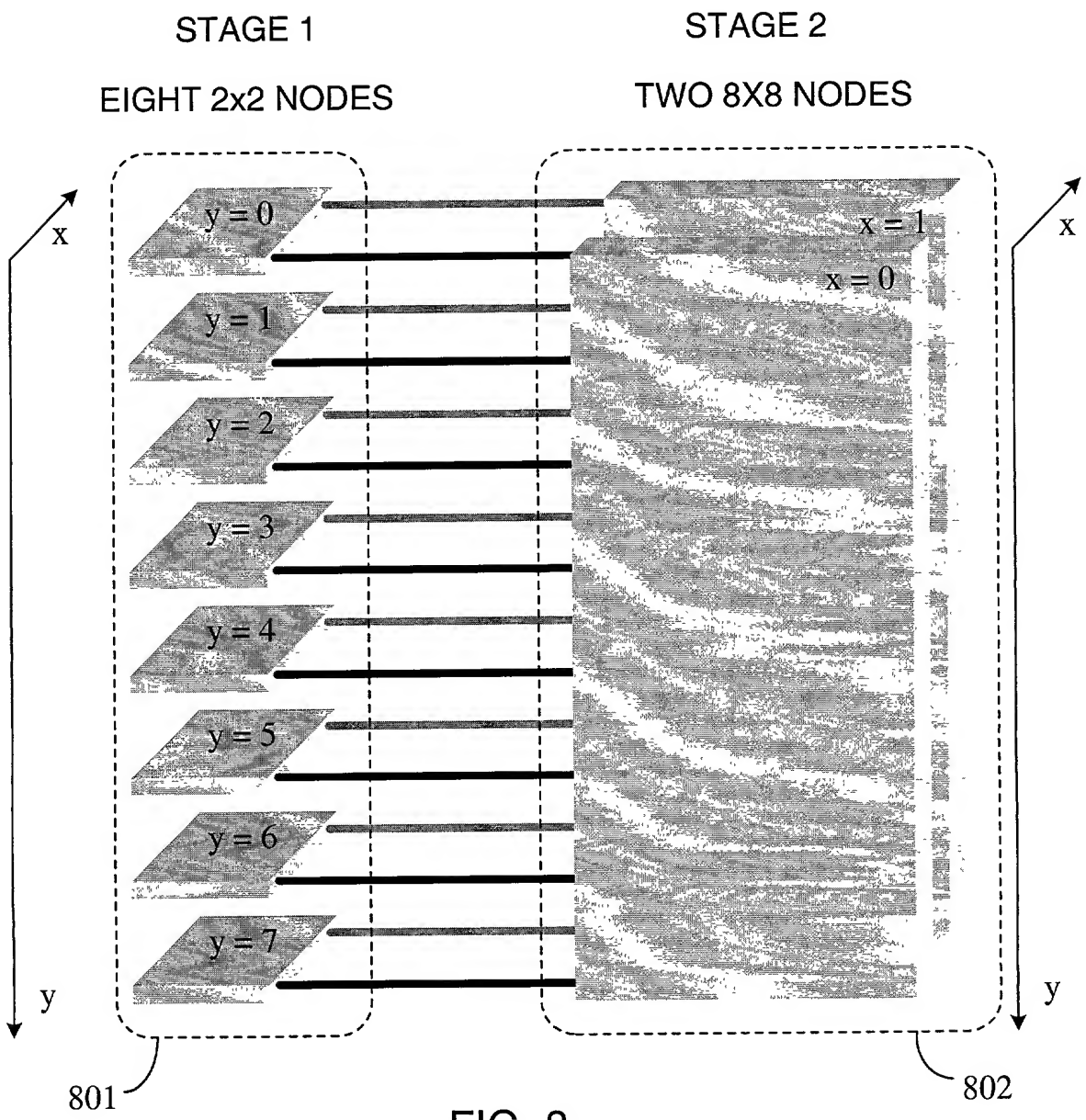


FIG. 8

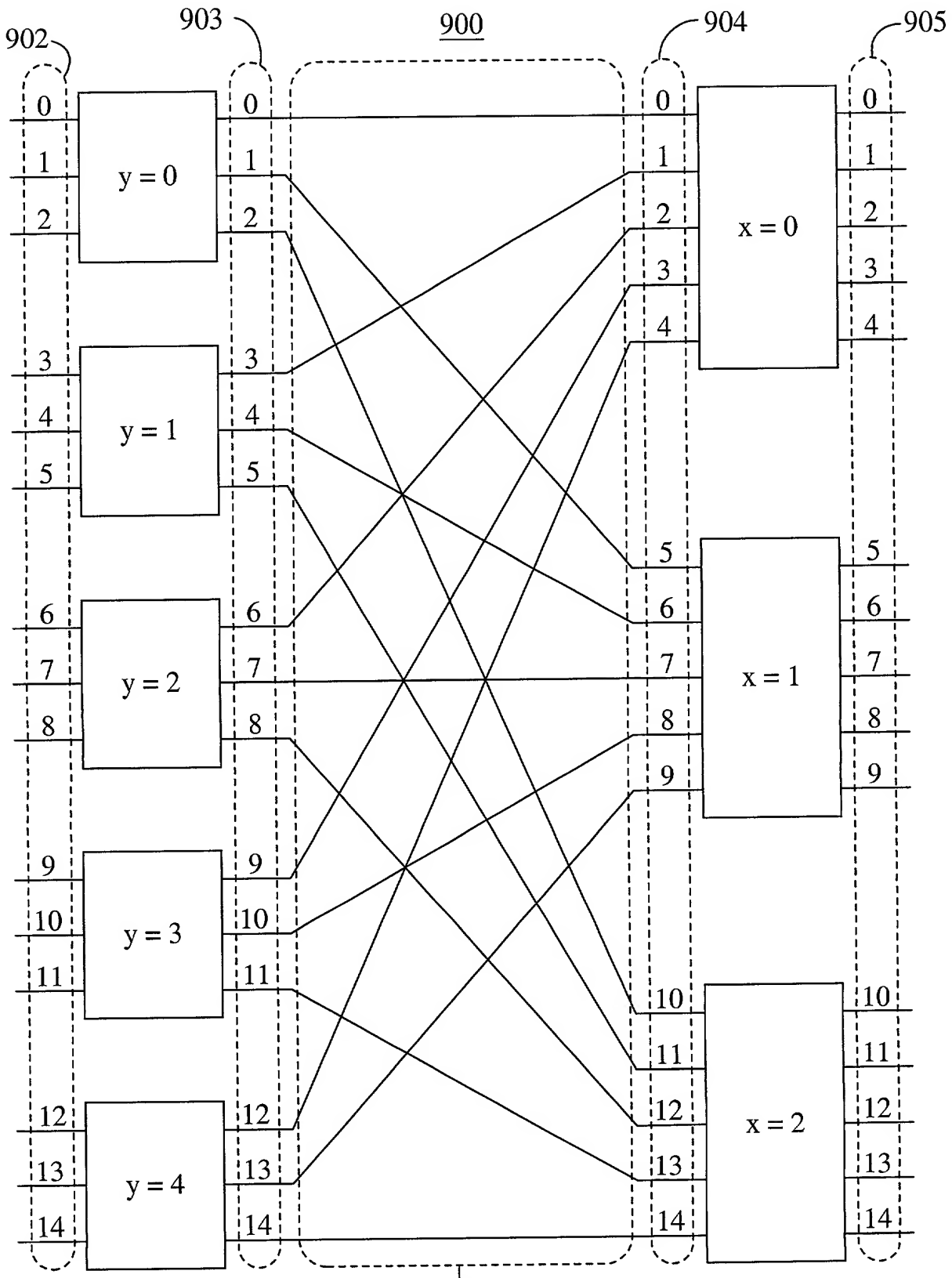


FIG. 9

US 6,925,469 B2

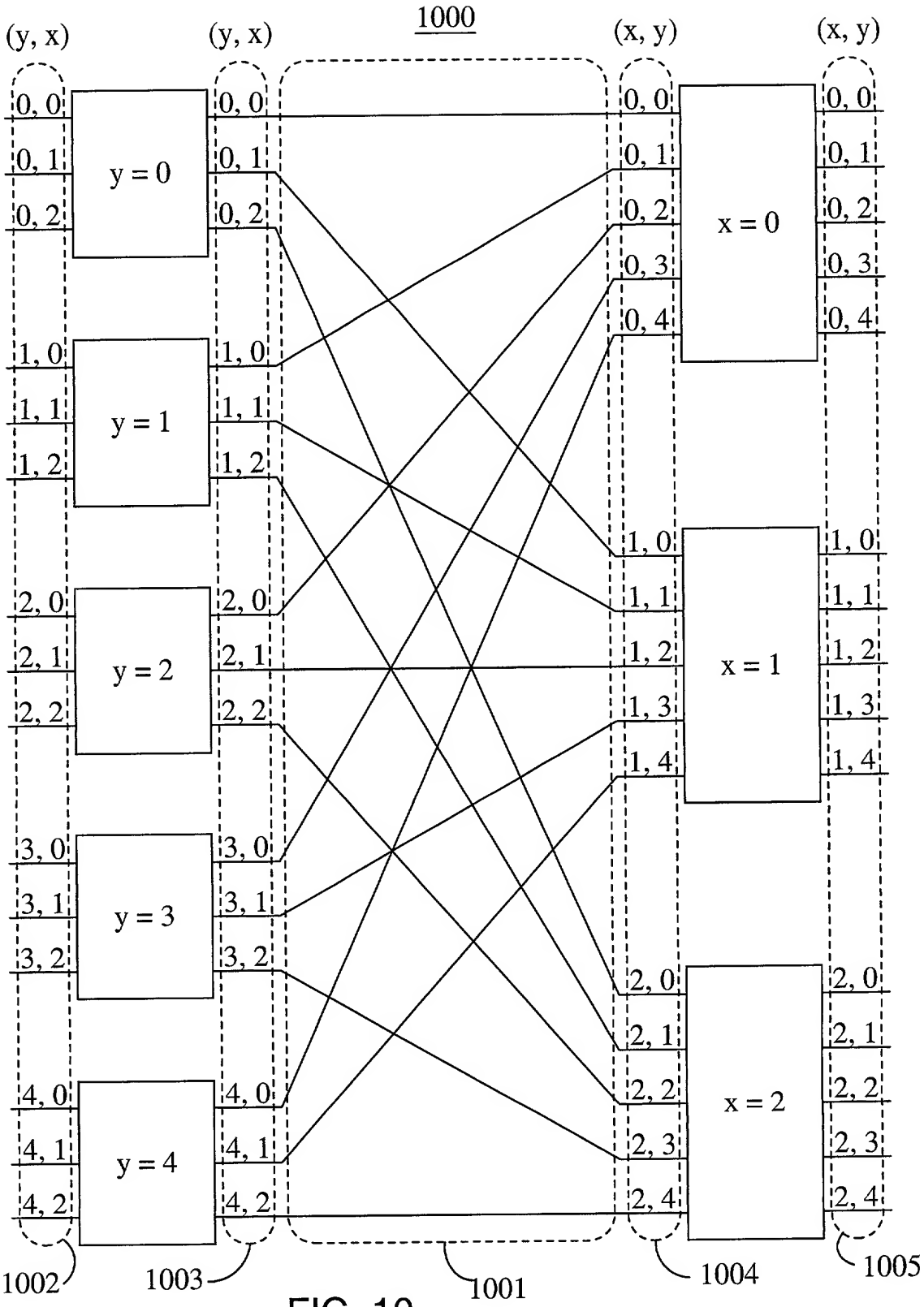


FIG. 10

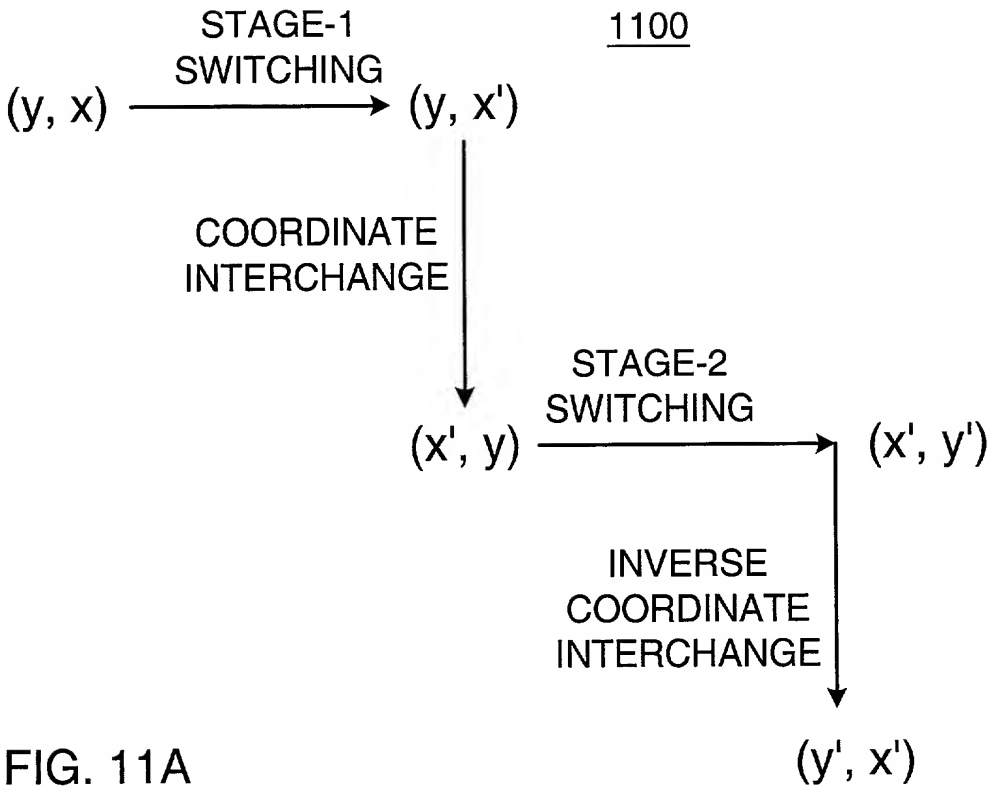


FIG. 11A

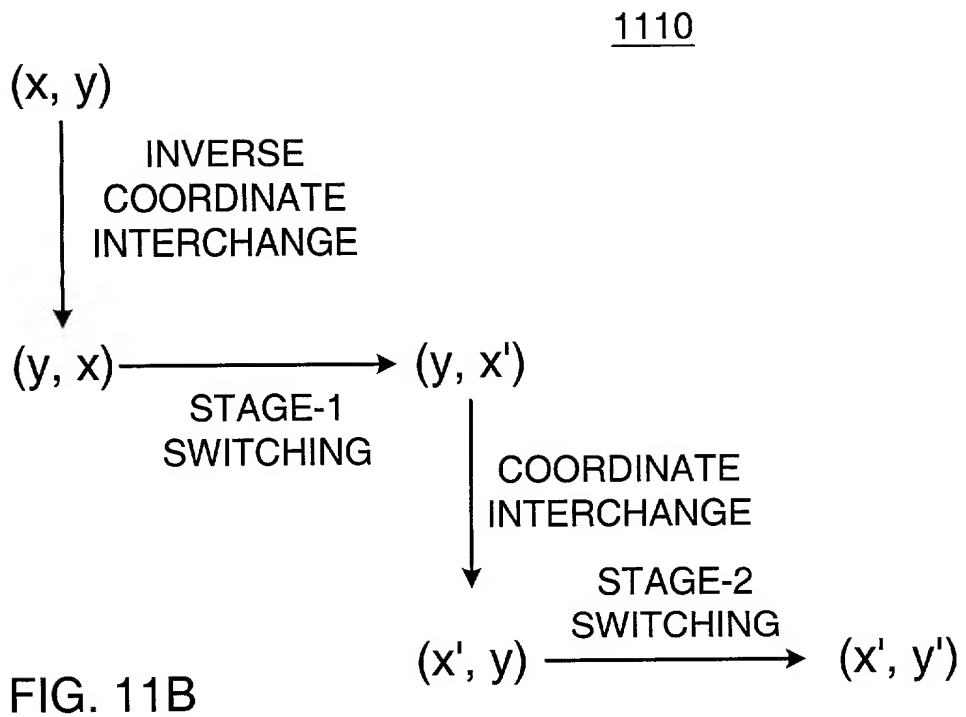
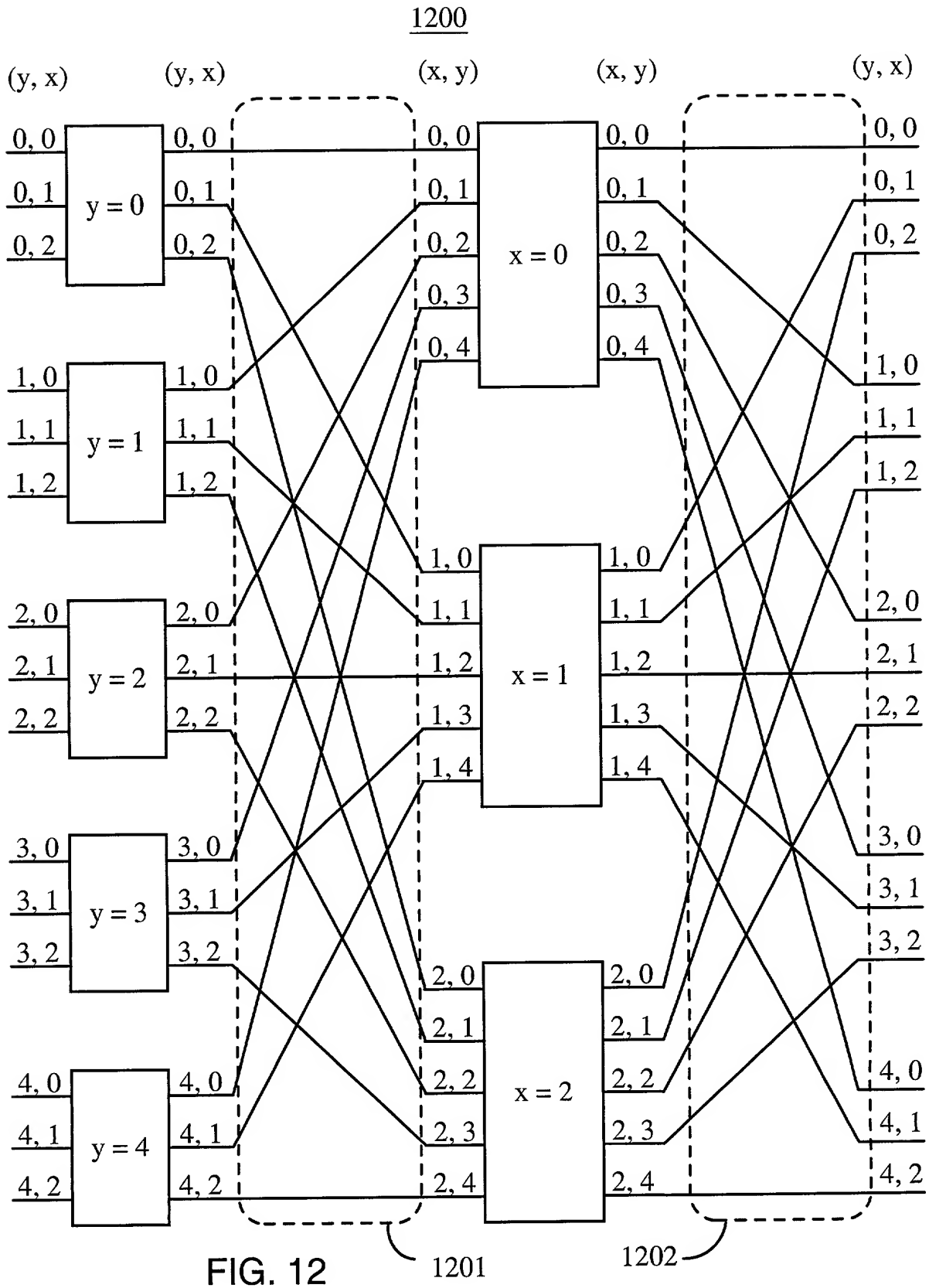


FIG. 11B

5,008,915 - 05/02/90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(y, x)
(x, y)
(x, y)
(y, x)
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1, 0
1, 1
1, 2
y = 1
2, 0
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2, 2
y = 2
3, 0
3, 1
3, 2
y = 3
4, 0
4, 1
4, 2
y = 4
0, 0
0, 1
0, 2
0, 3
0, 4
x = 0
1, 0
1, 1
1, 2
1, 3
1, 4
x = 1
2, 0
2, 1
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2, 3
2, 4
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1201
1202

FIG. 12

US 9,294,450 B2

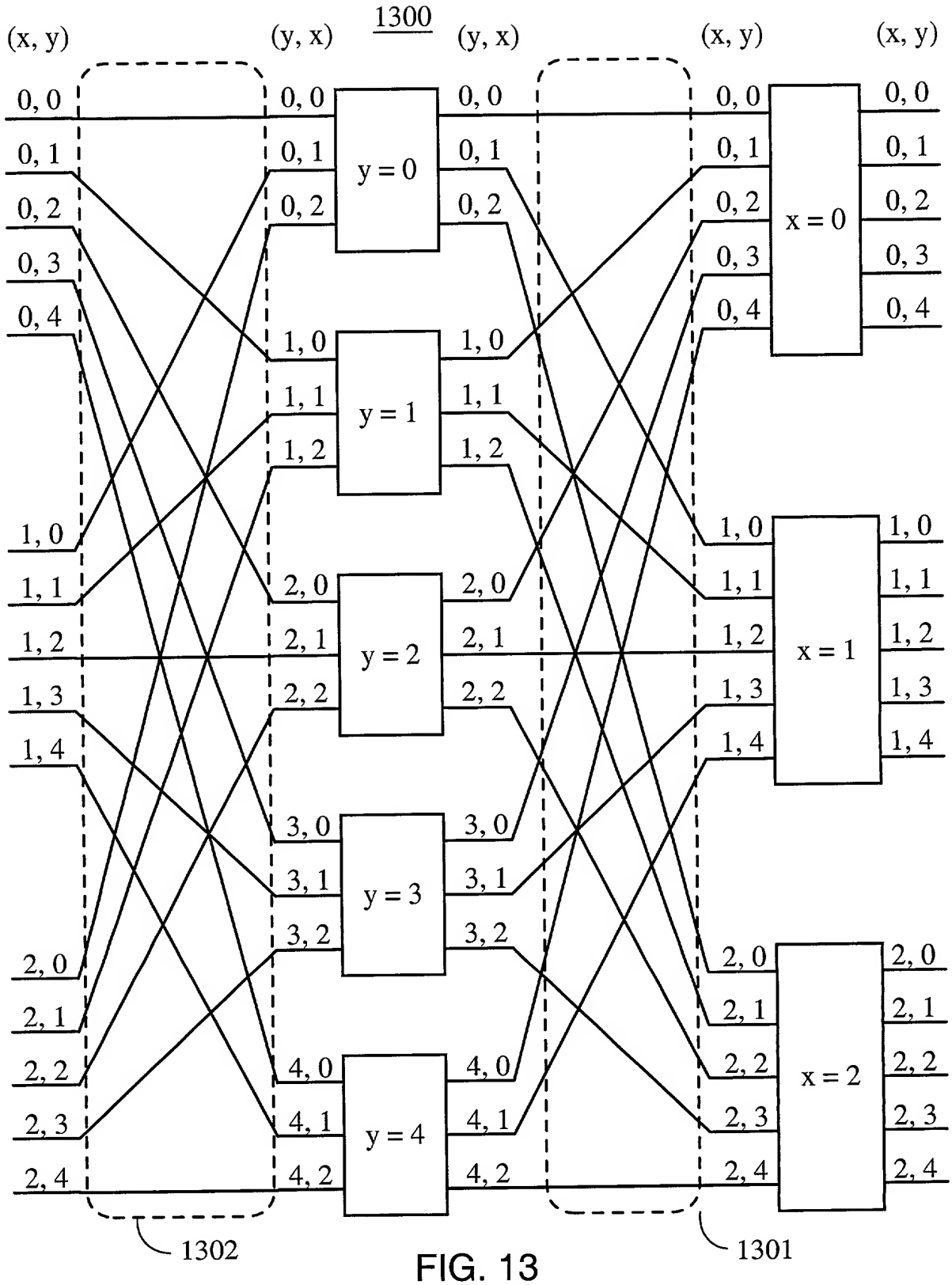

FIG. 13

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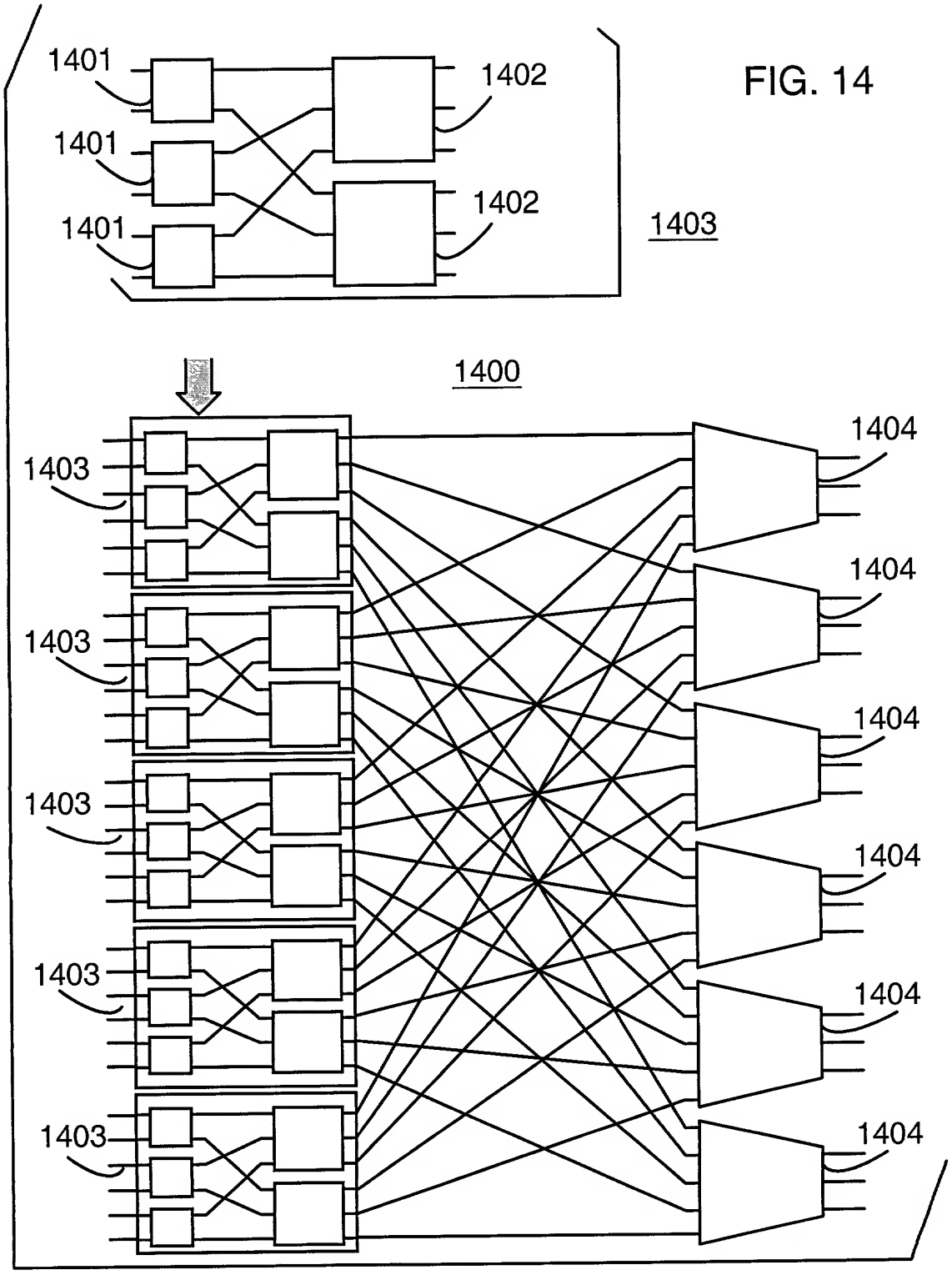


FIG. 14

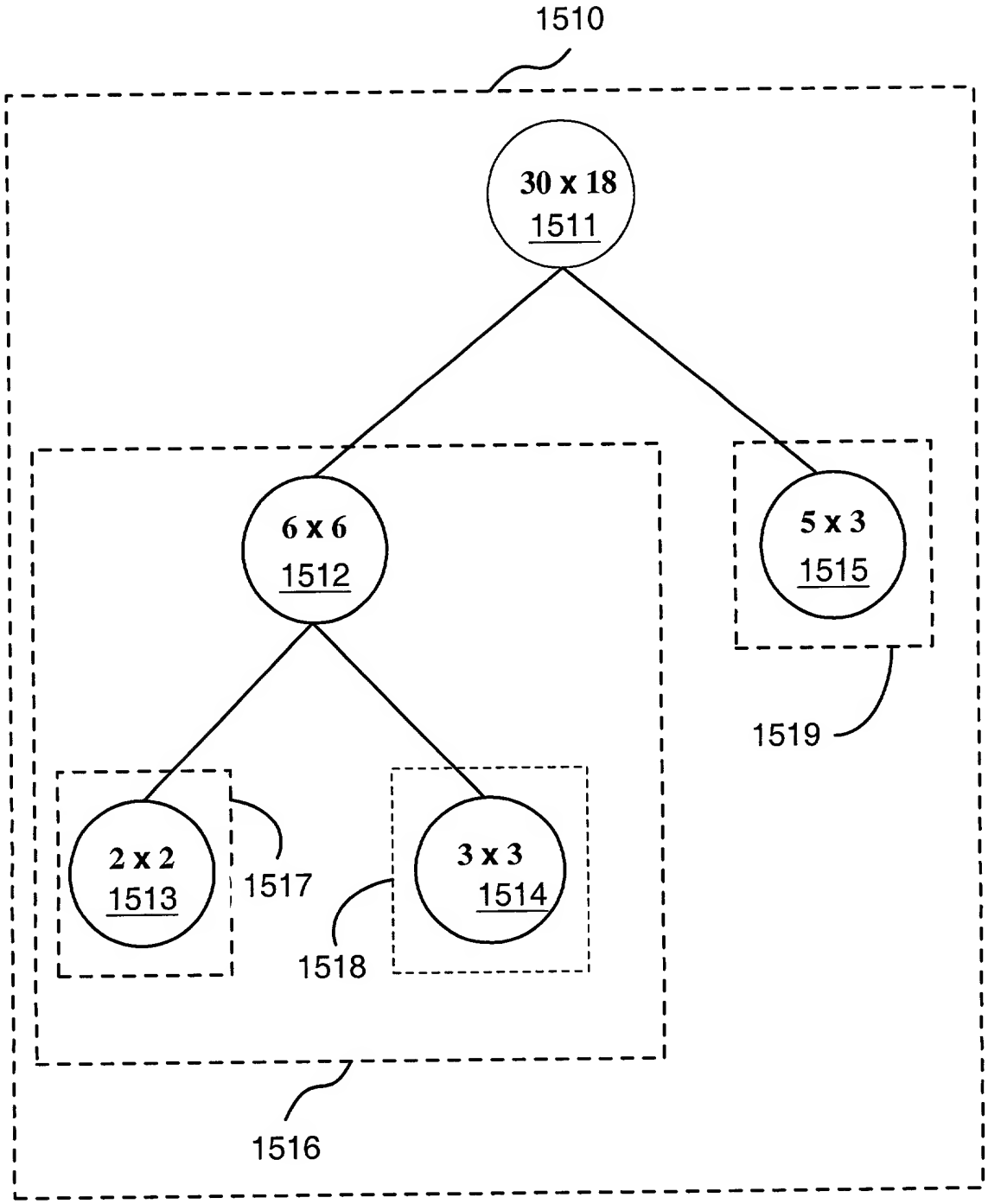


FIG. 15

US 6,826,297 B2

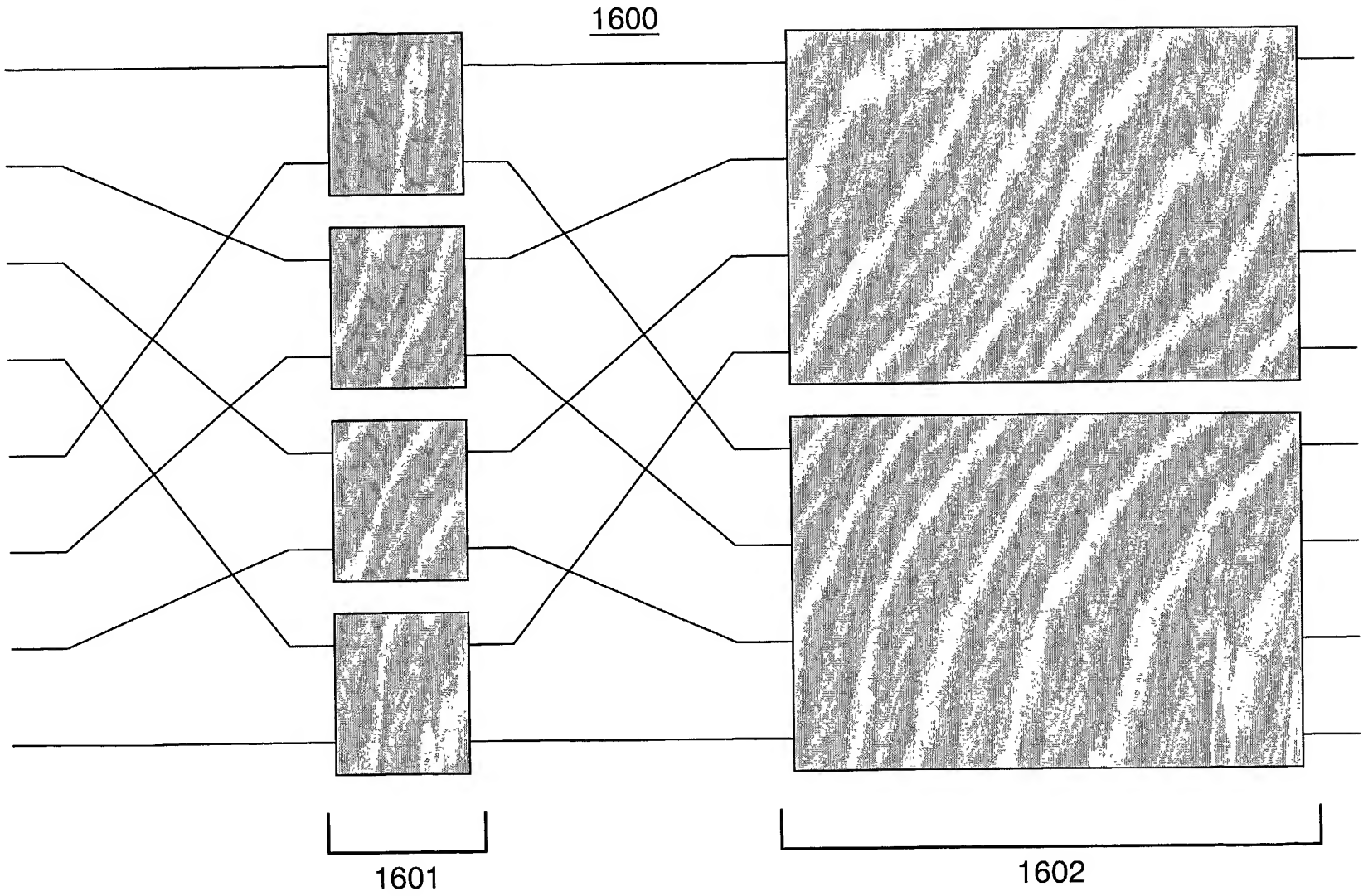


FIG. 16

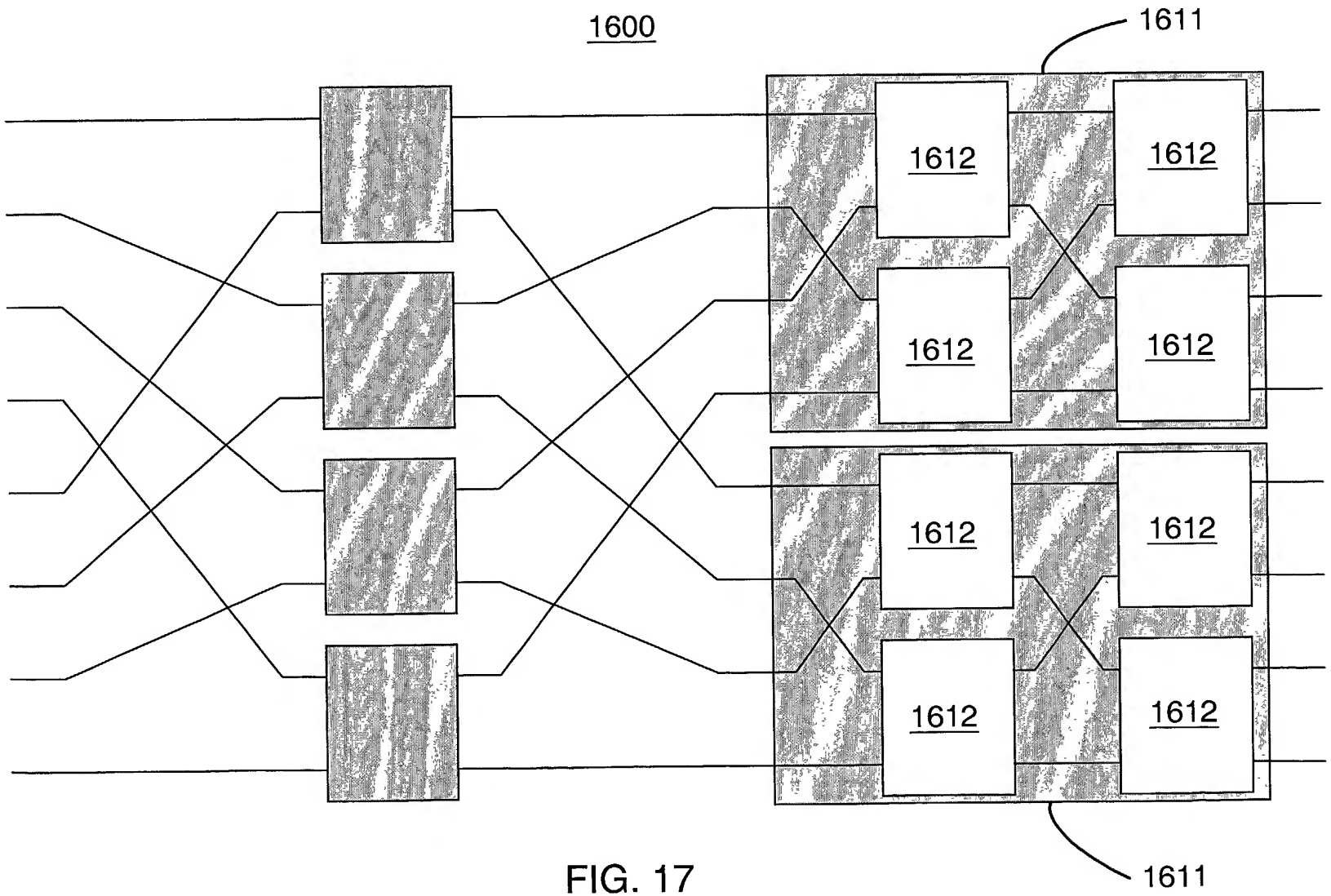
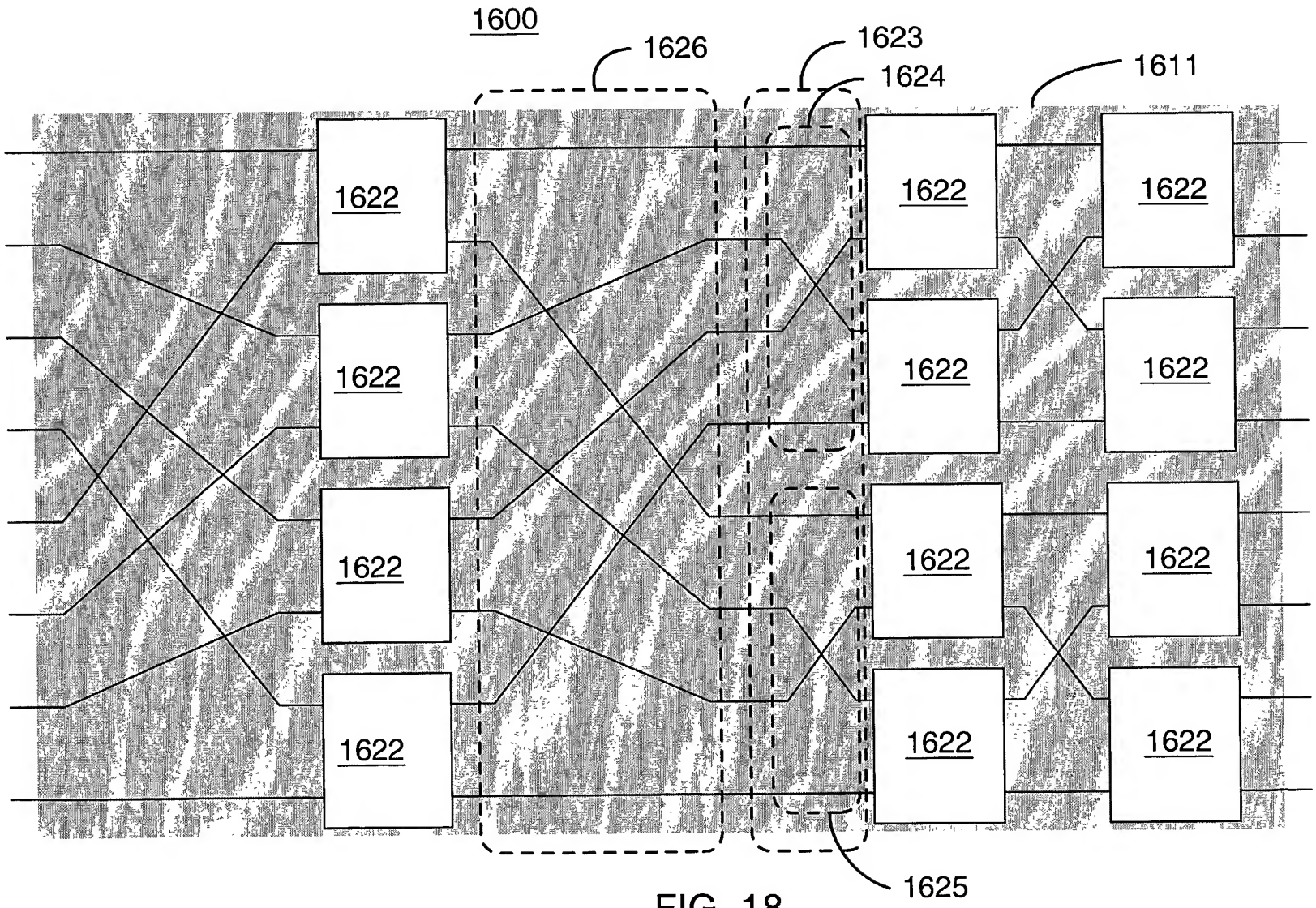


FIG. 17


1600
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1625

FIG. 18

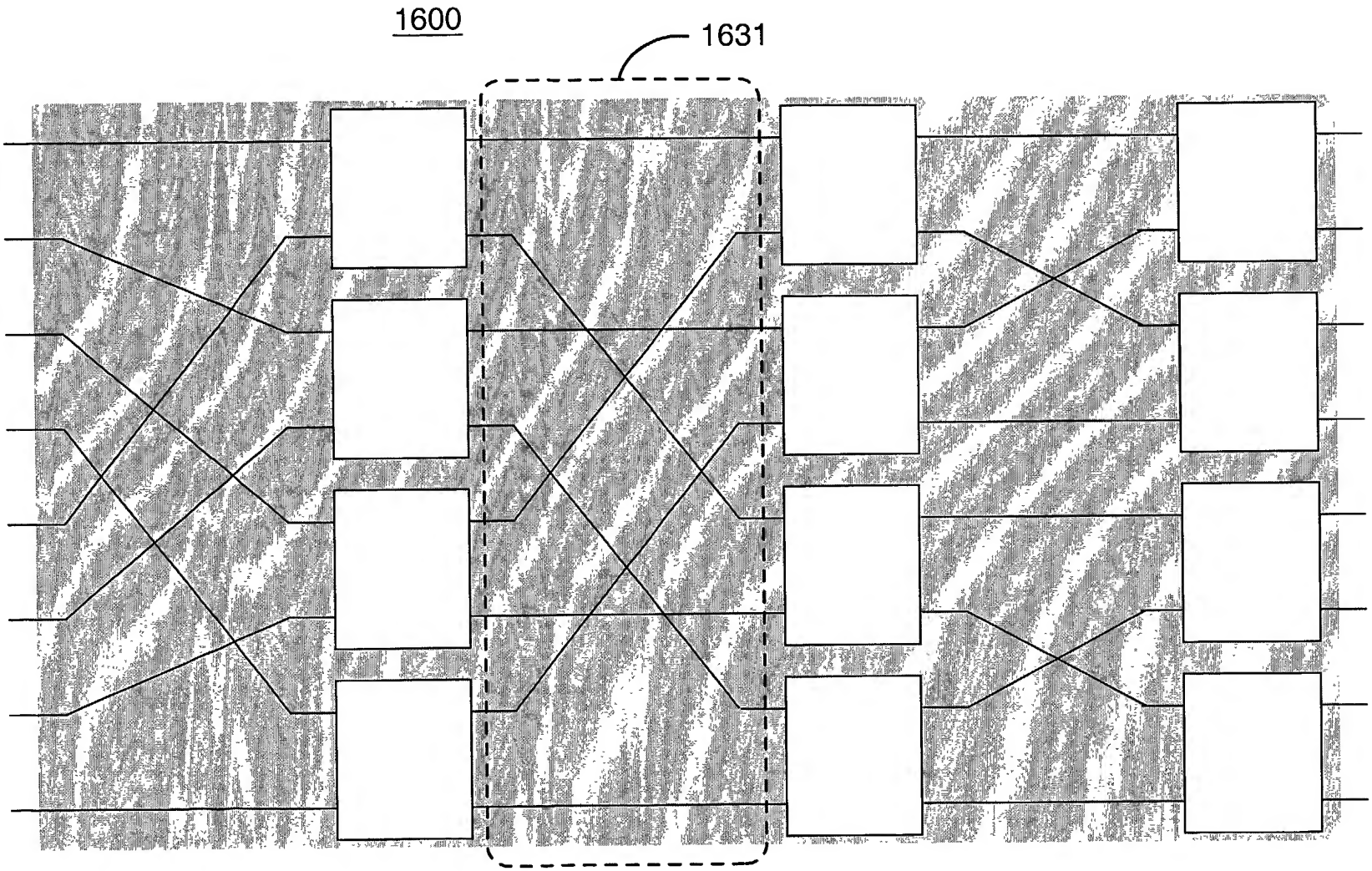


FIG. 19

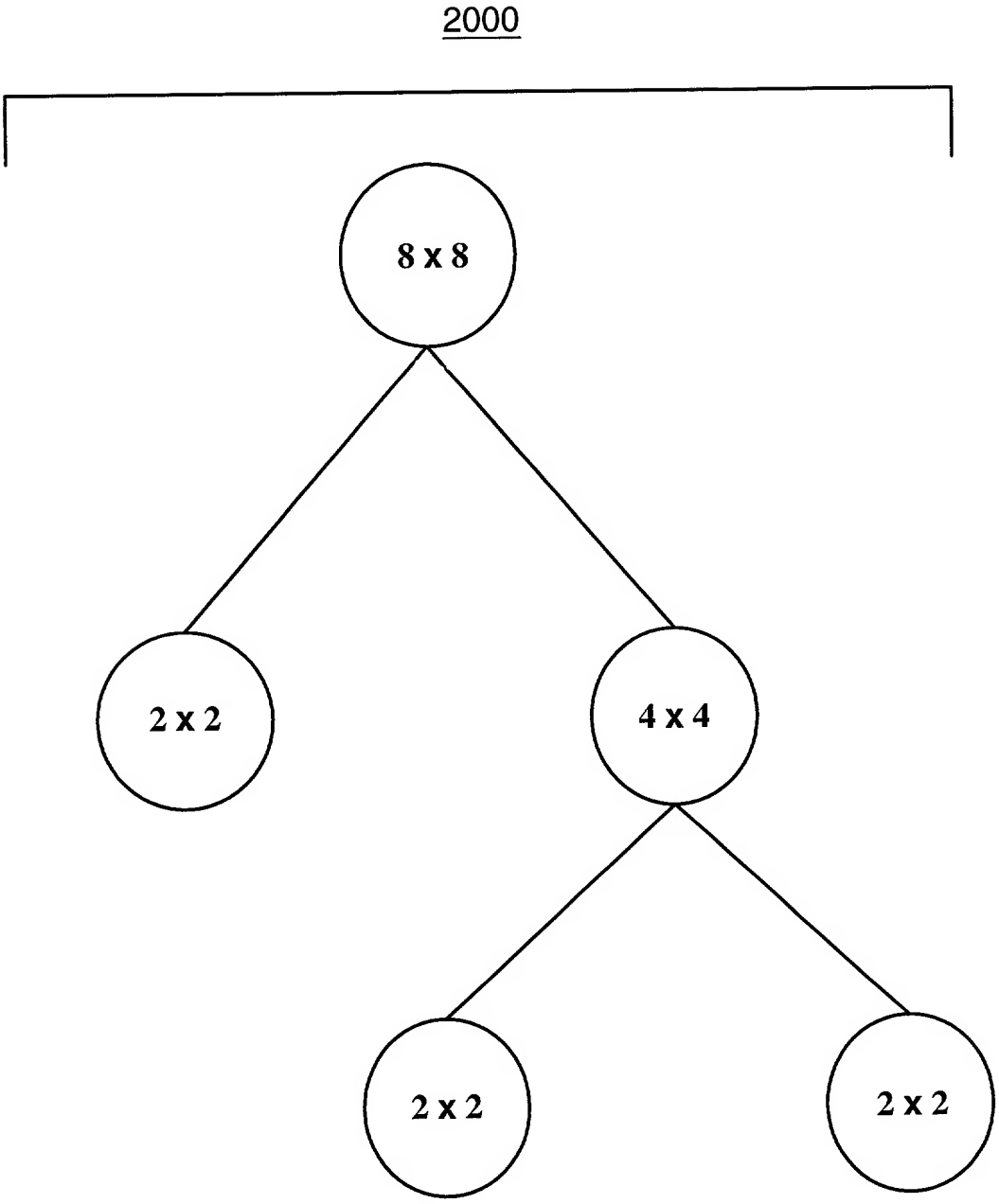


FIG. 20

20020120 5448260 A1

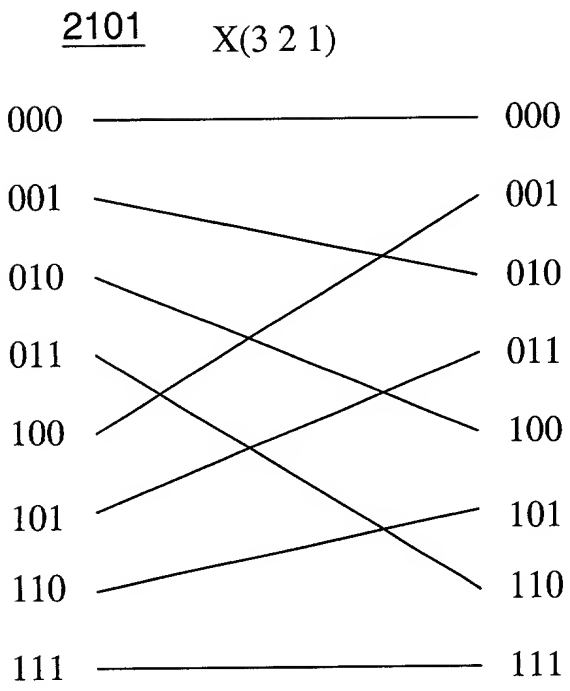


FIG. 21A

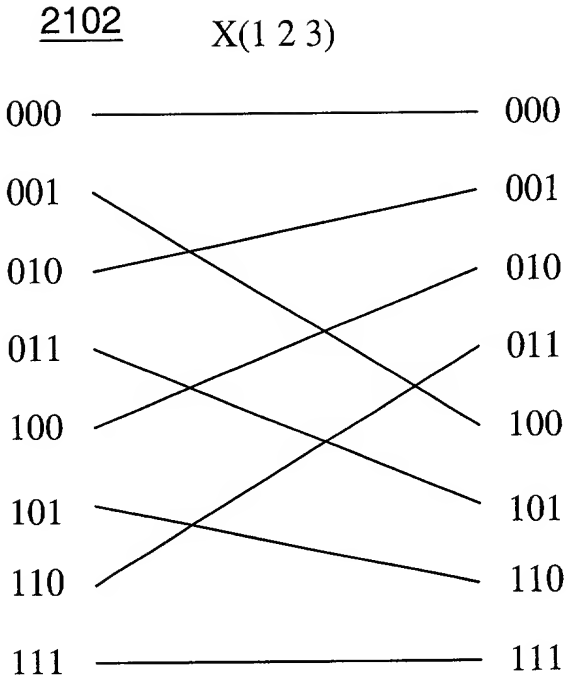


FIG. 21B

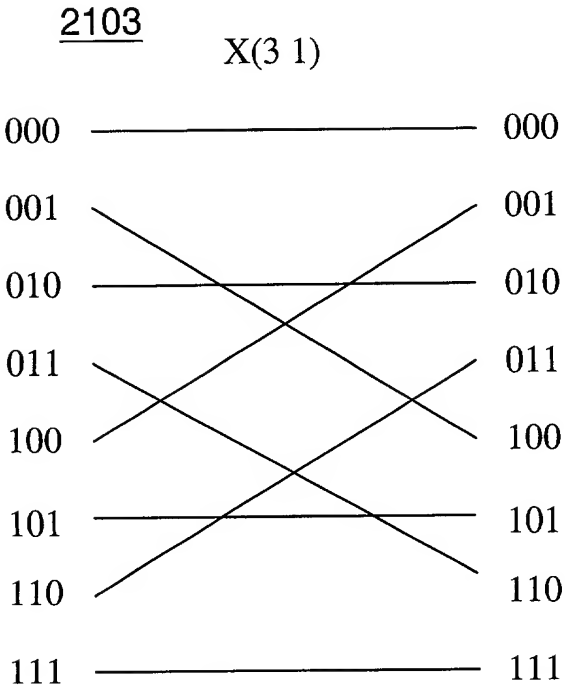


FIG. 21C

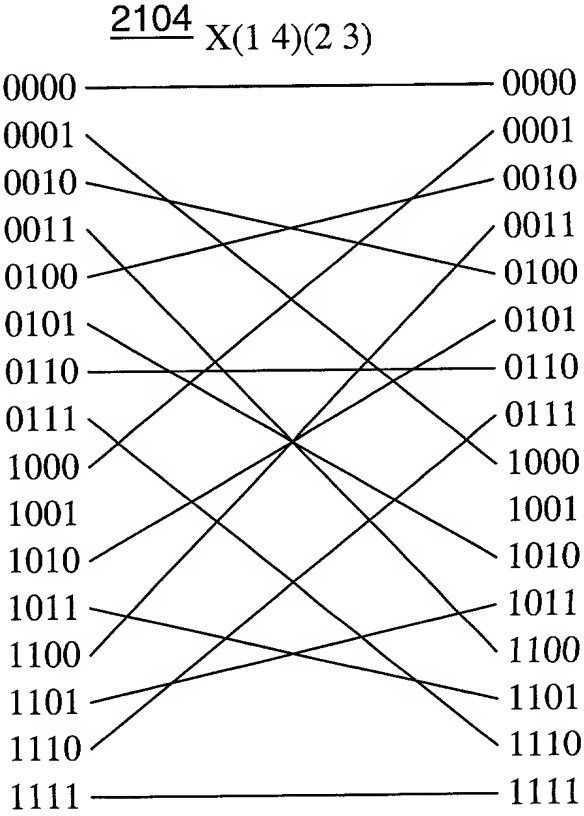
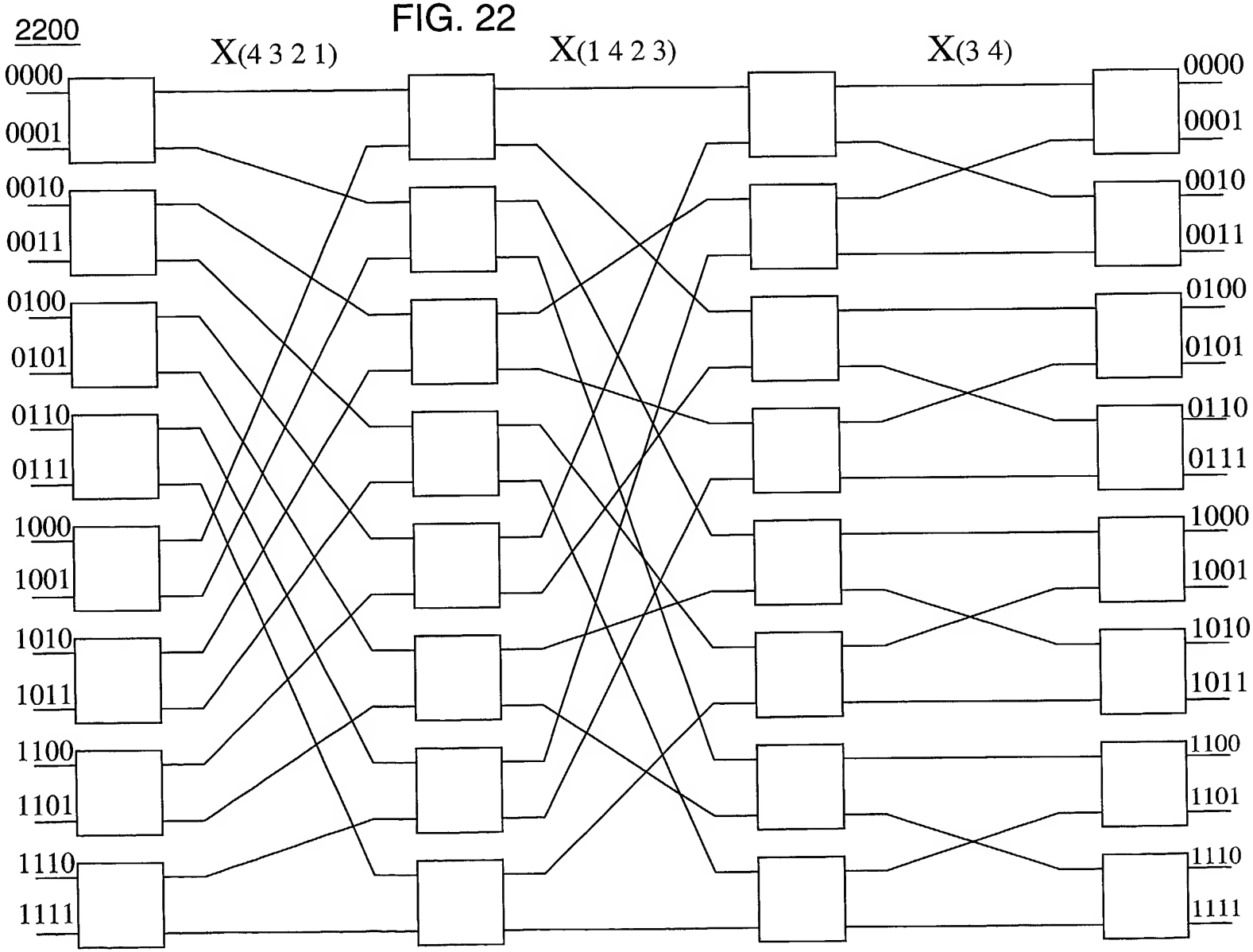


FIG. 21D

FIG. 22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X(1 4 2 3)
X(3 4)
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0010
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0100
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0110
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1001
1010
1011
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1101
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0011
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1001
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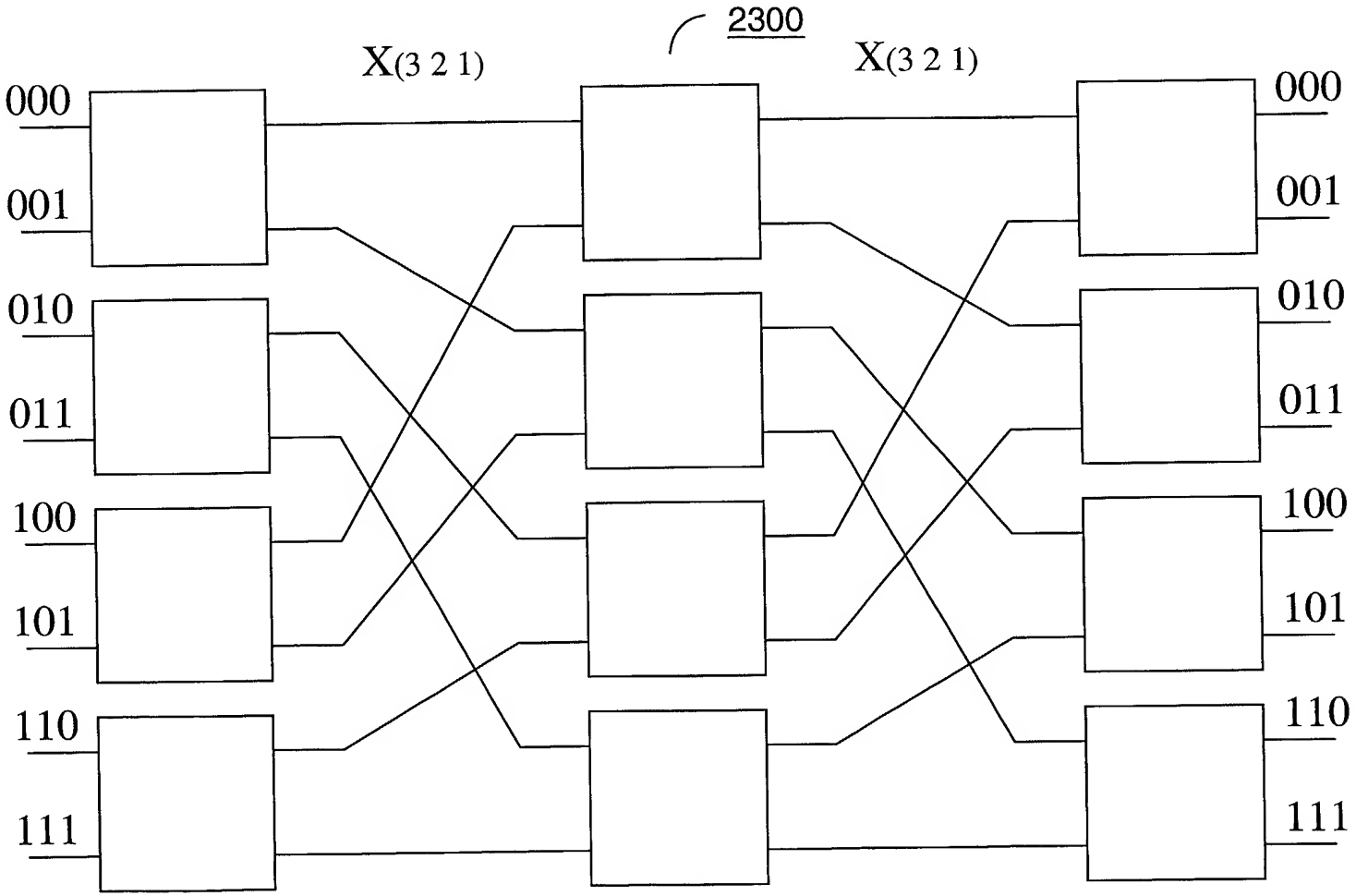
1100
1101
1110
1111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X(3 2 1)
X(3 2 1)
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111
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011
100
101
110
111

FIG. 23

2400

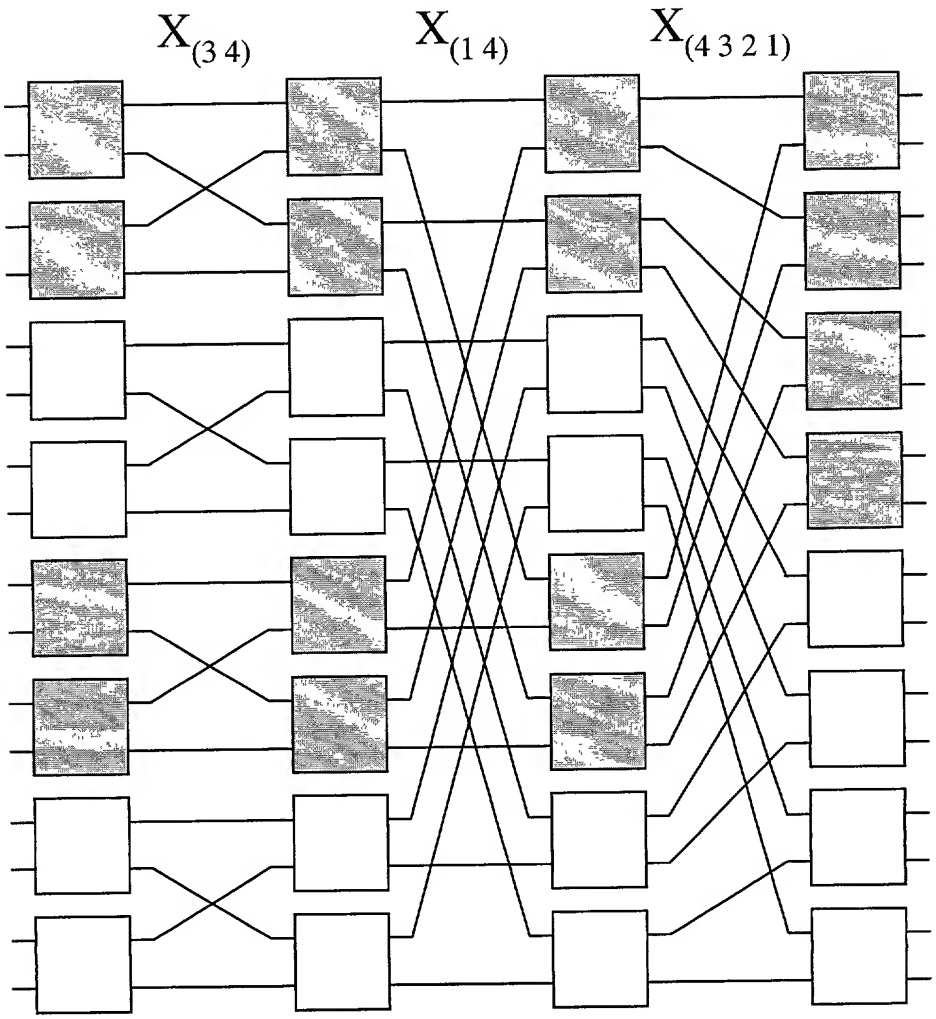


FIG. 24

FIG. 25

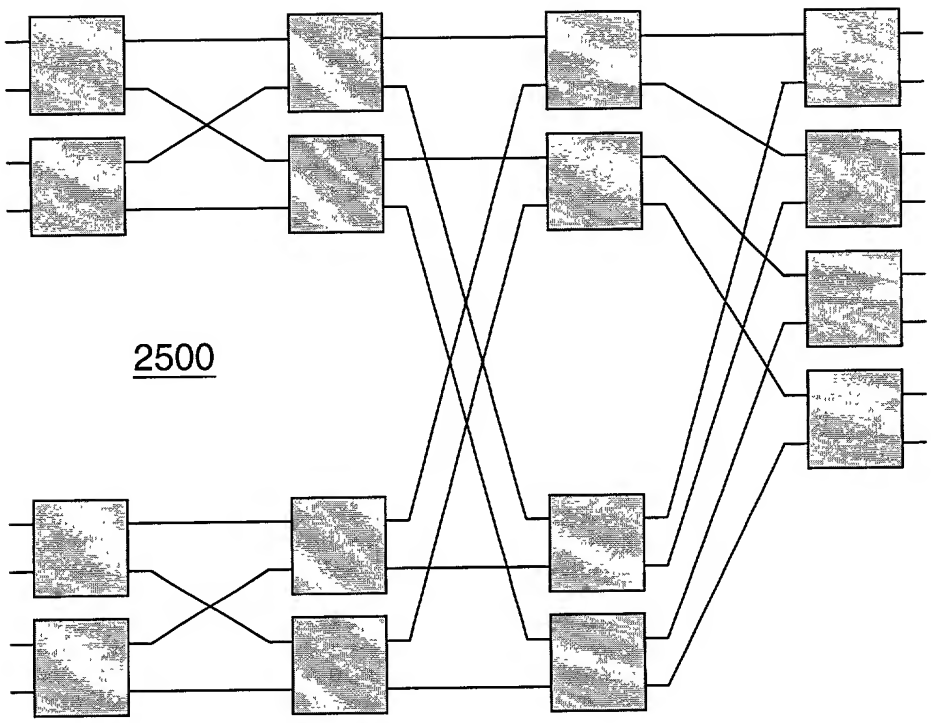
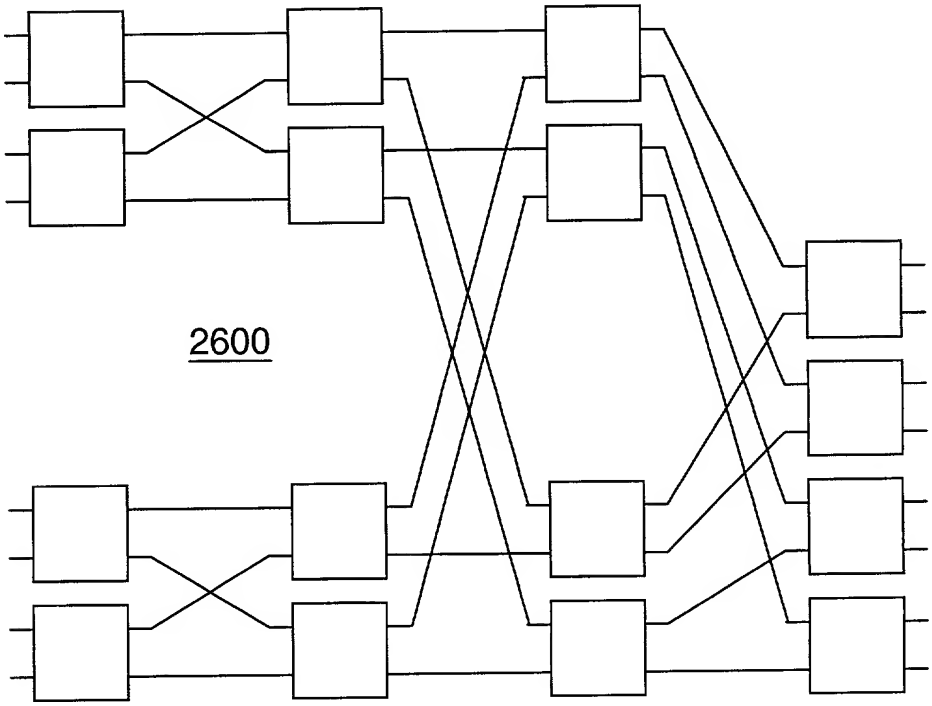


FIG. 26



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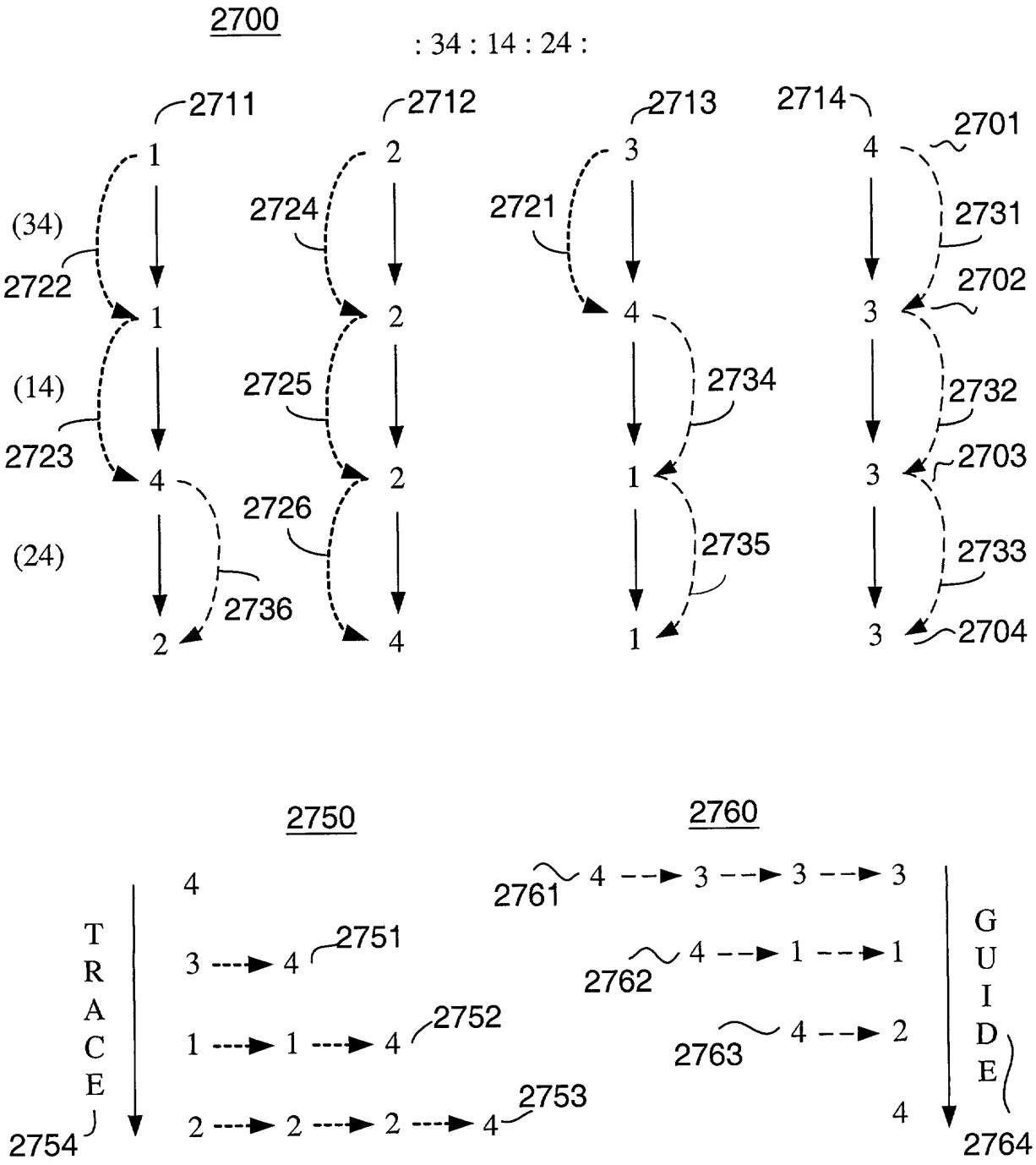
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FIG. 27

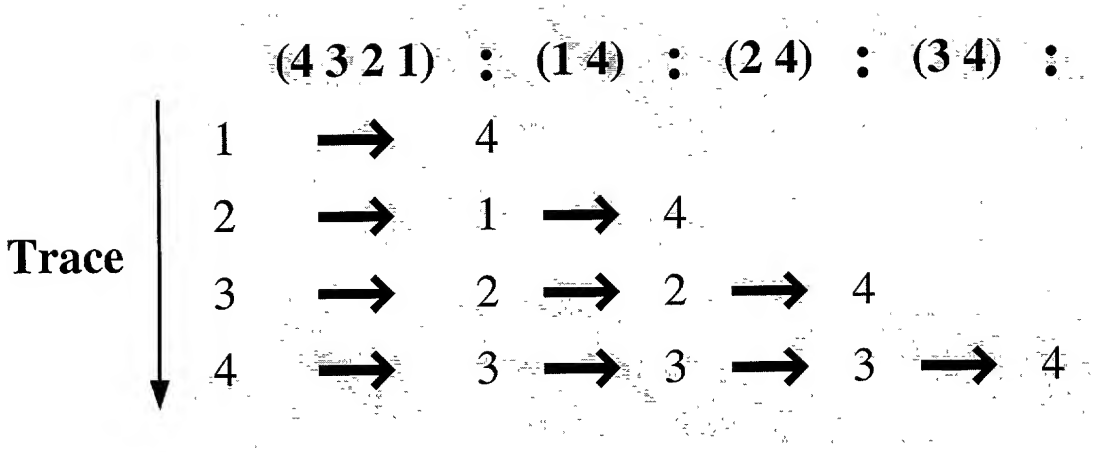

FIG. 28A

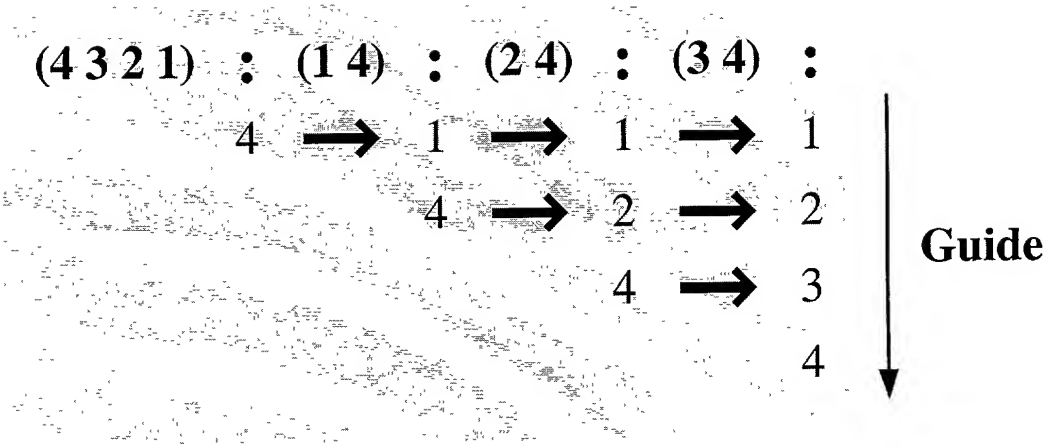

FIG. 28B

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FIG. 29

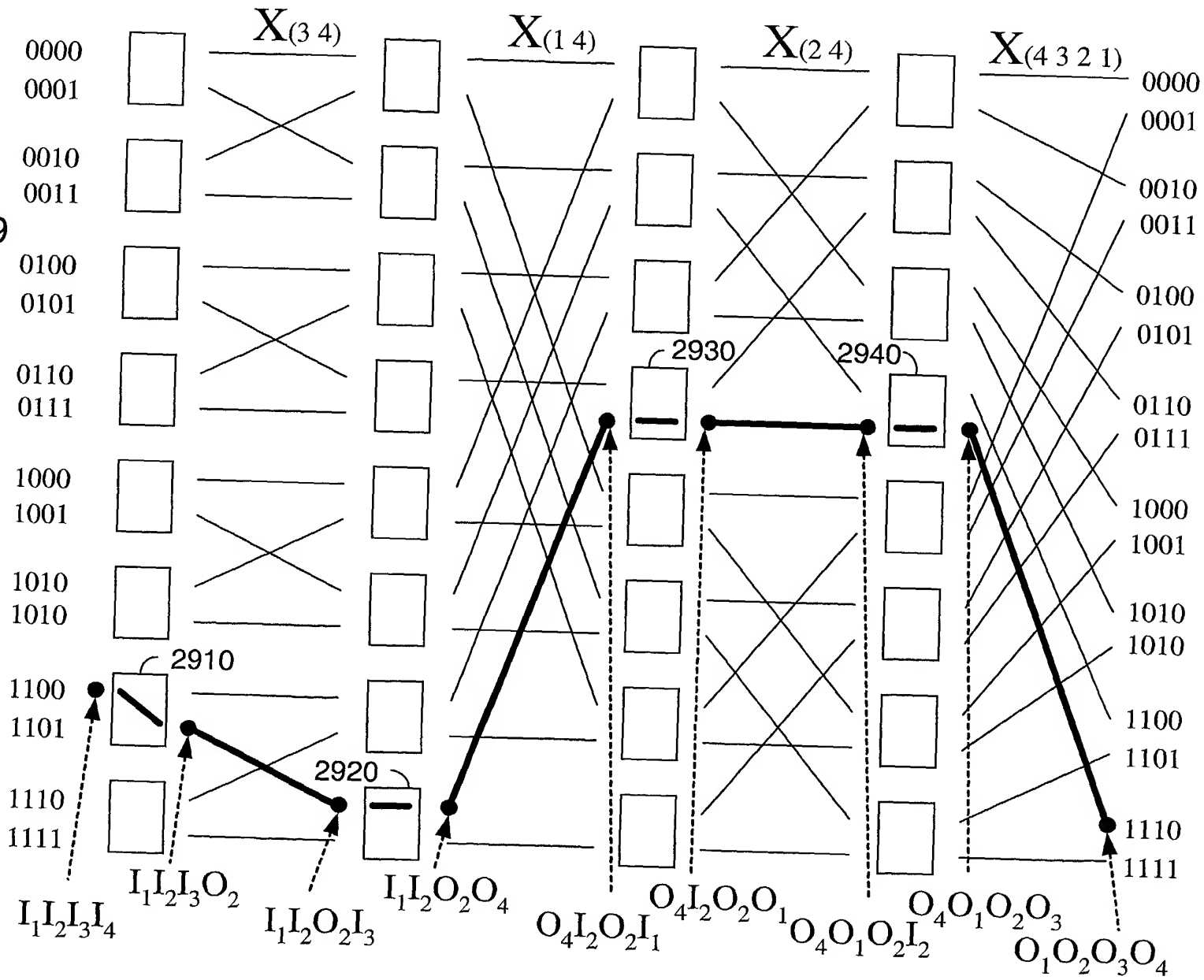


FIG. 30A

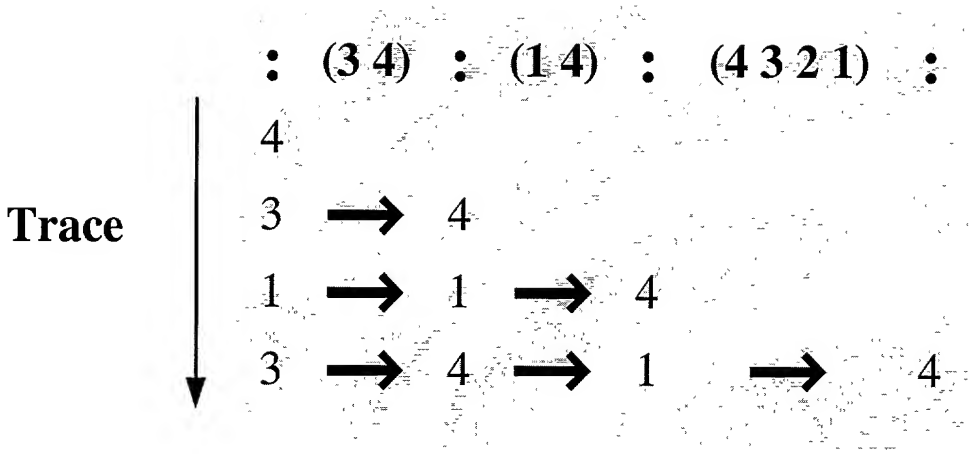
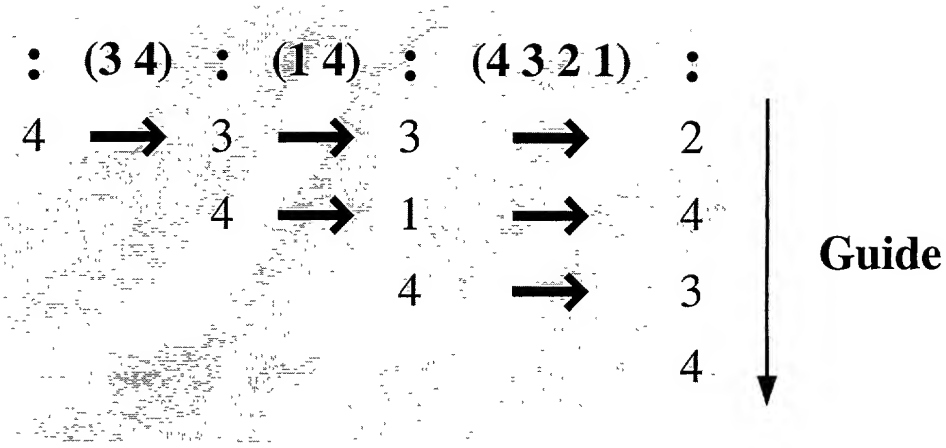


FIG. 30B



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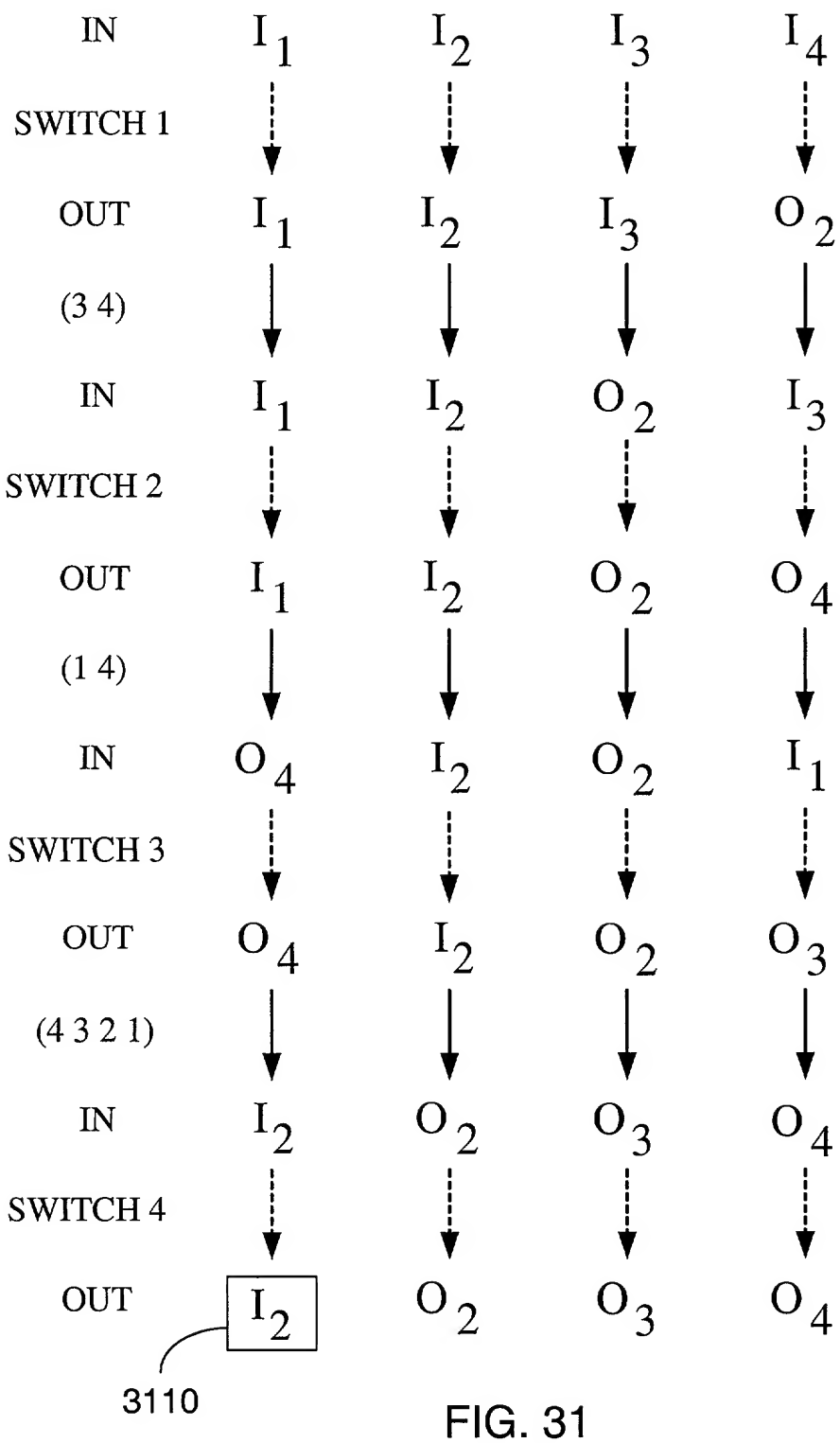


FIG. 31

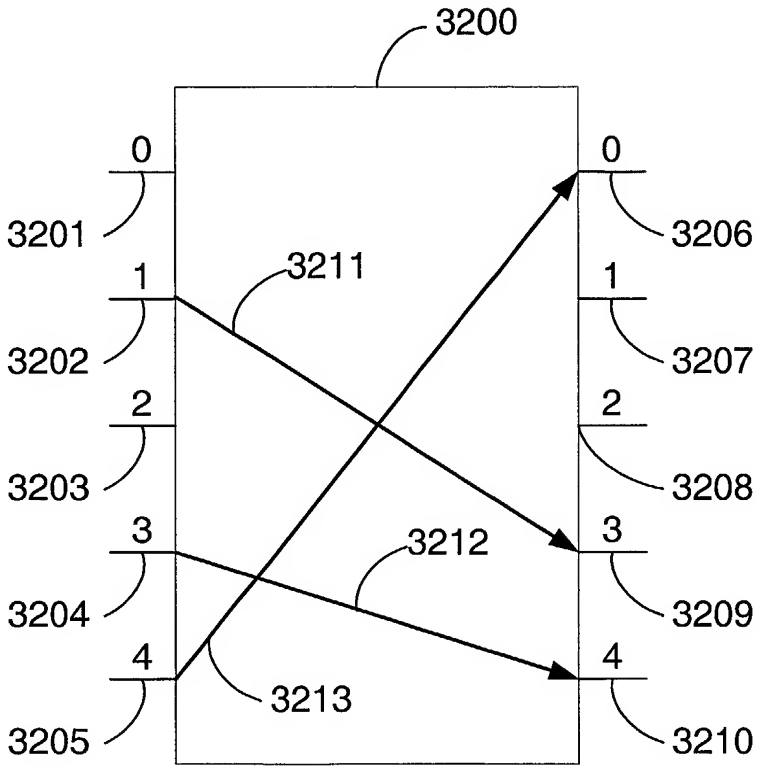


FIG. 32A

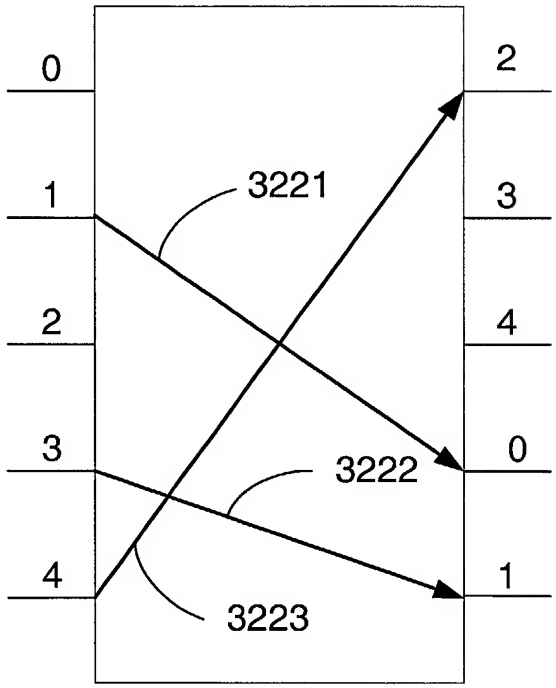


FIG. 32B

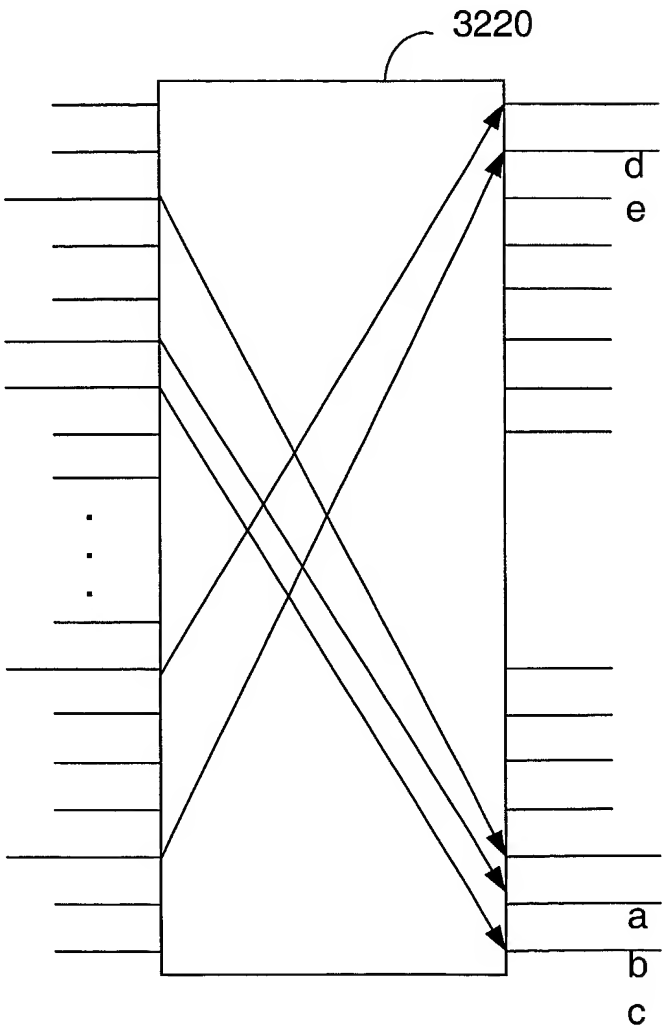


FIG. 32C

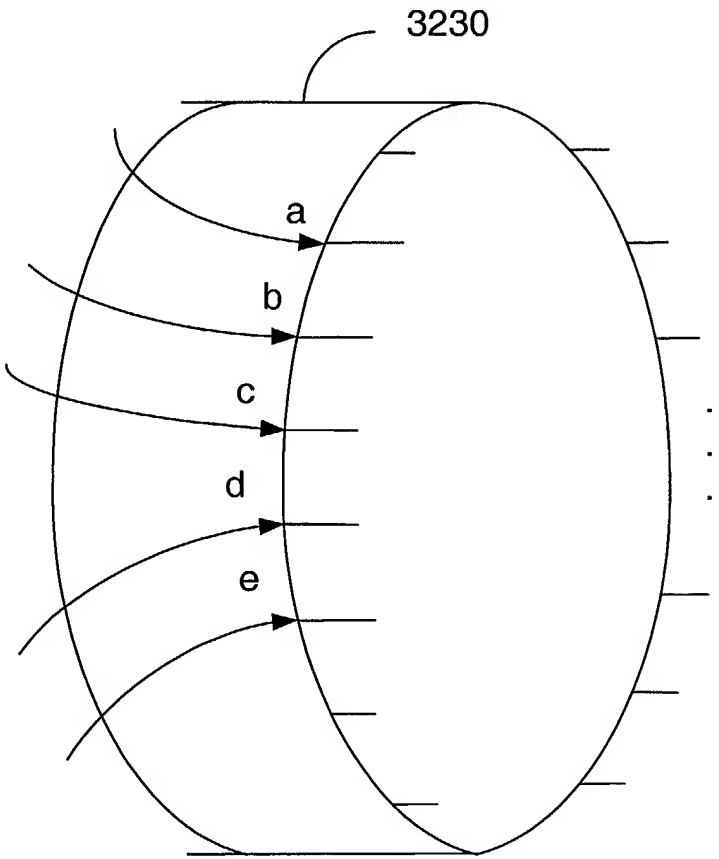


FIG. 32D

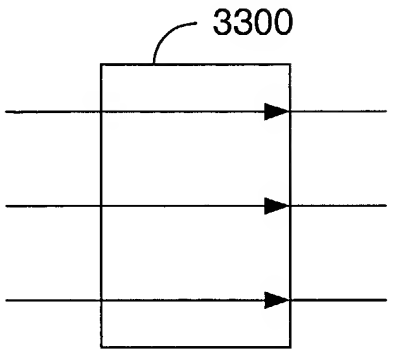


FIG. 33A

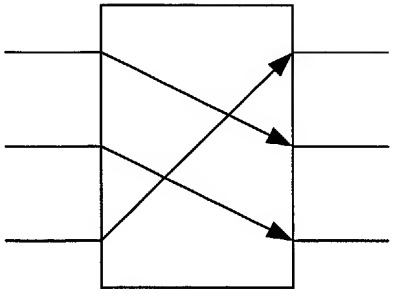


FIG. 33B

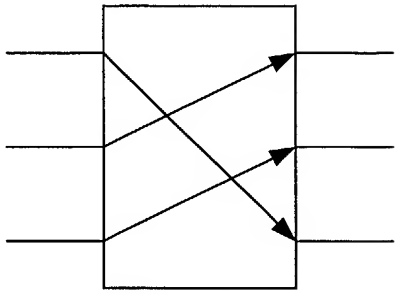


FIG. 33C

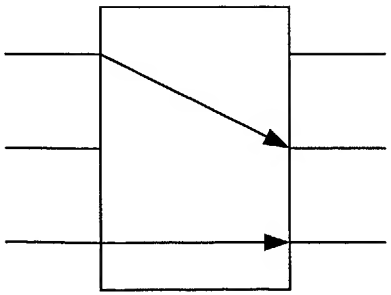


FIG. 33D

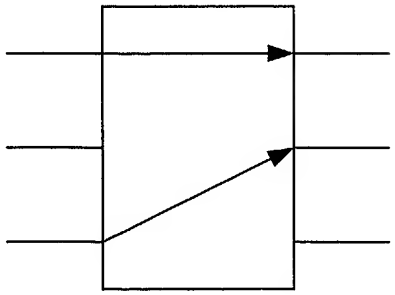


FIG. 33E

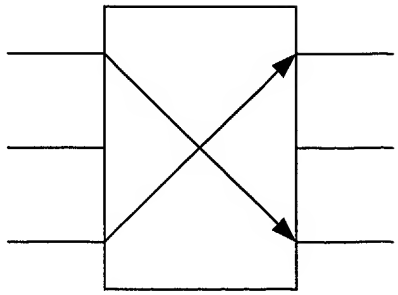


FIG.33F

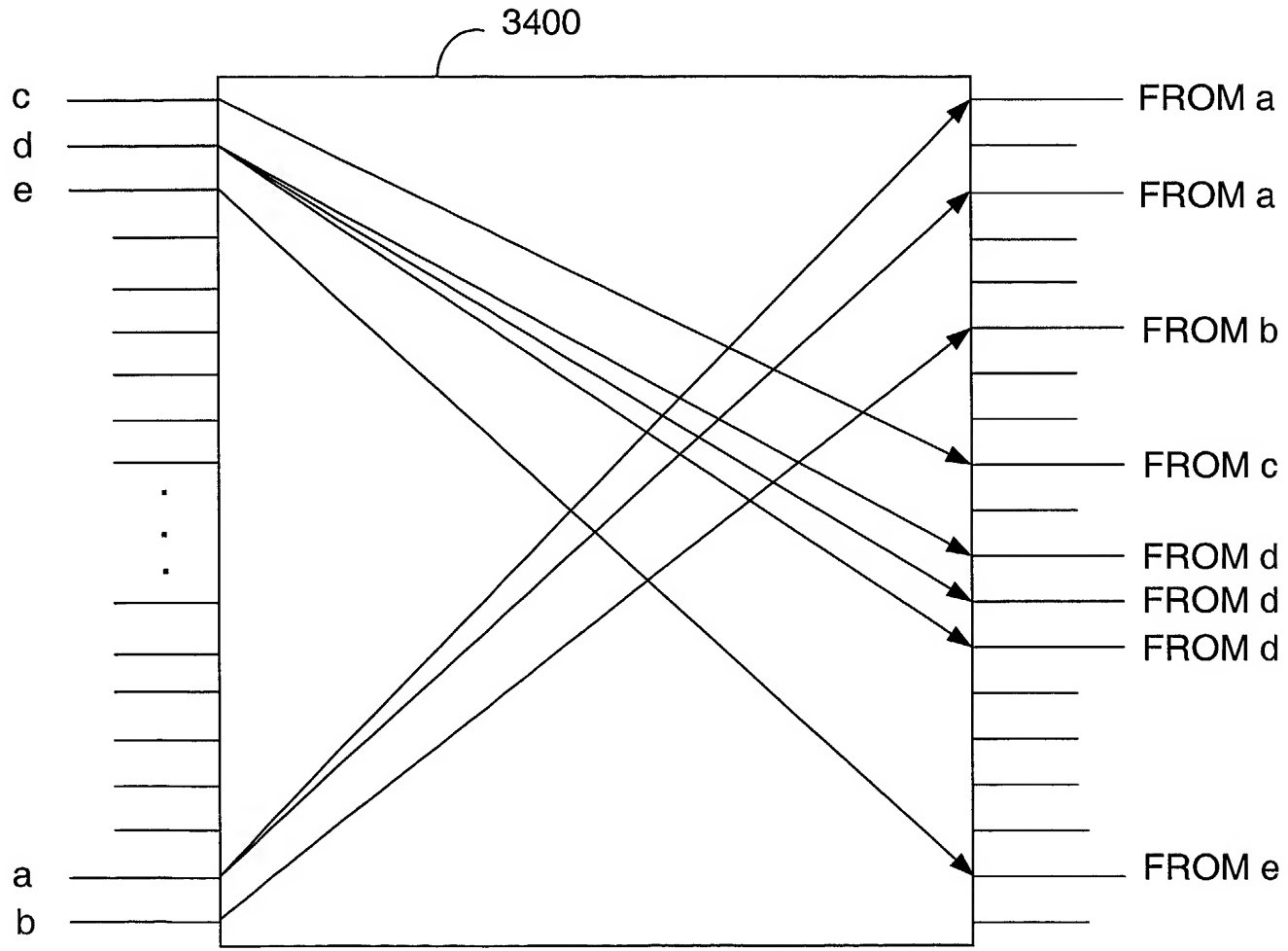


FIG. 34

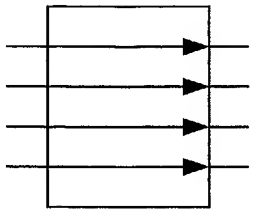


FIG. 35A

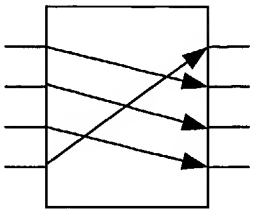


FIG. 35B

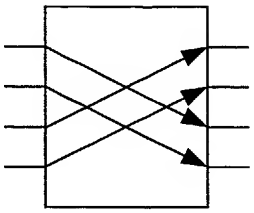


FIG. 35C

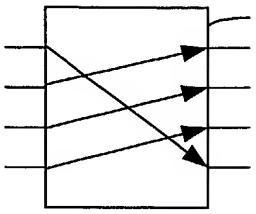


FIG. 35D

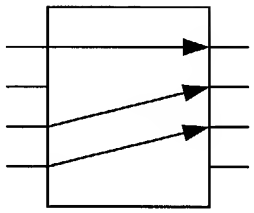


FIG. 35E

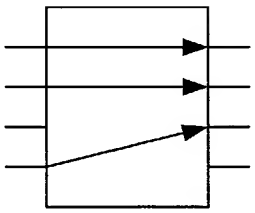


FIG. 35F

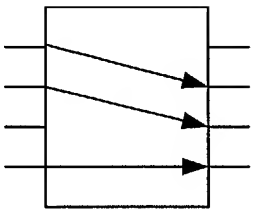


FIG. 35G

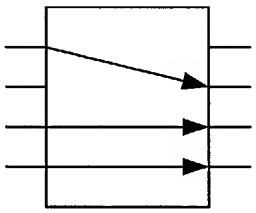


FIG. 35H

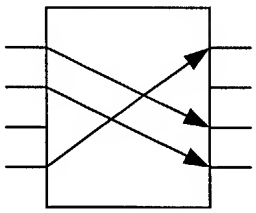


FIG. 35I

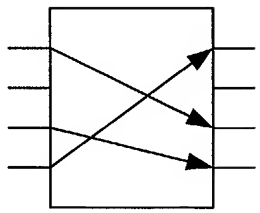


FIG. 35J

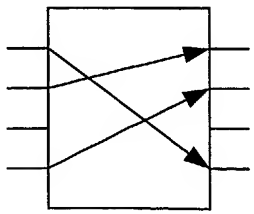


FIG. 35K

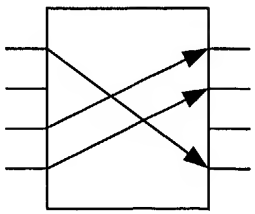


FIG. 35L

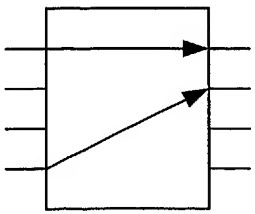


FIG. 35M

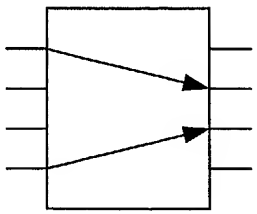


FIG. 35N

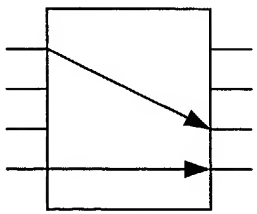


FIG. 35O

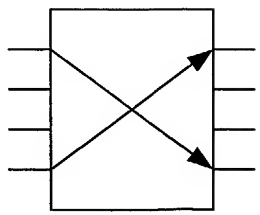


FIG. 35P

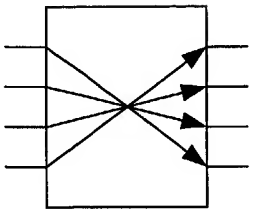


FIG. 36A

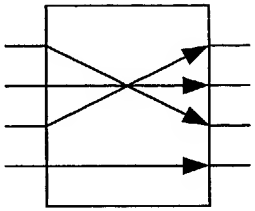


FIG. 36B

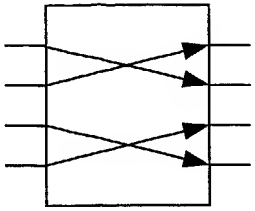


FIG. 36C

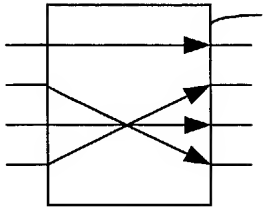


FIG. 36D

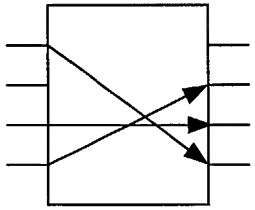


FIG. 36E

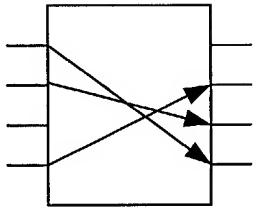


FIG. 36F

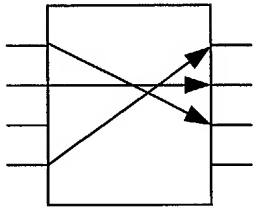


FIG. 36G

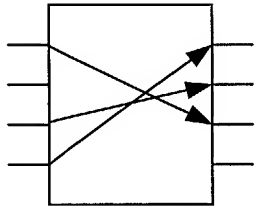


FIG. 36H

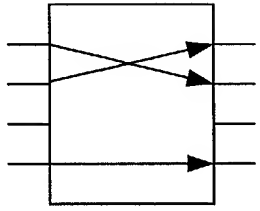


FIG. 36I

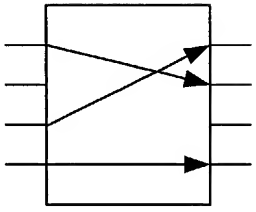


FIG. 36J

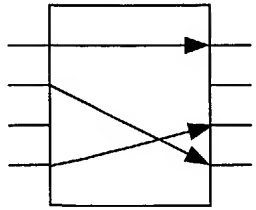


FIG. 36K

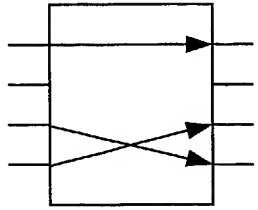


FIG. 36L

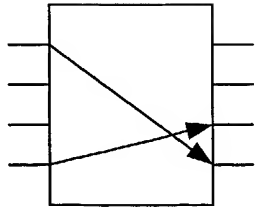


FIG. 36M

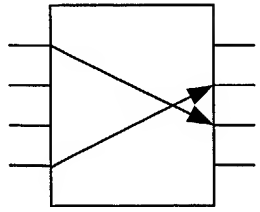


FIG. 36N

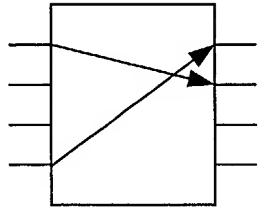


FIG. 36O

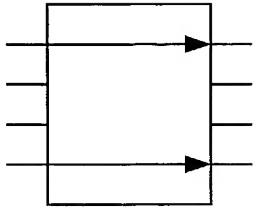


FIG. 36P

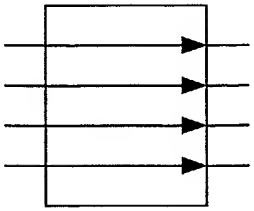


FIG. 37A

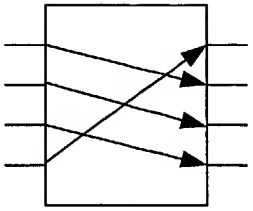


FIG. 37B

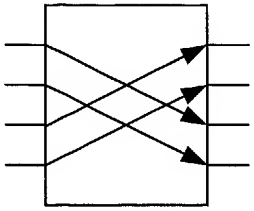


FIG. 37C

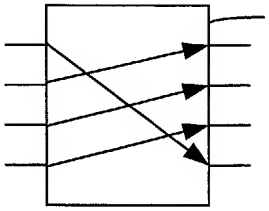


FIG. 37D

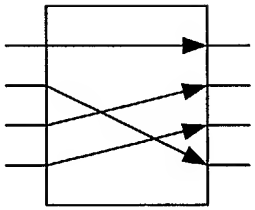


FIG. 37E

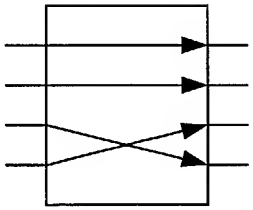


FIG. 37F

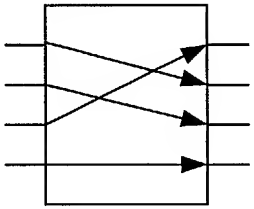


FIG. 37G

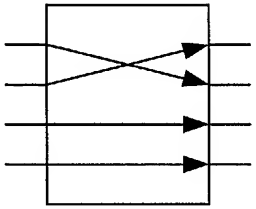


FIG. 37H

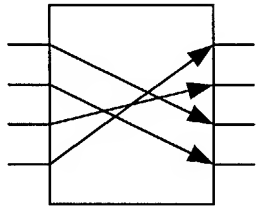


FIG. 37I

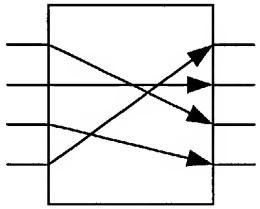


FIG. 37J

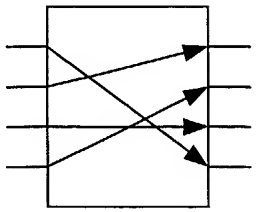


FIG. 37K

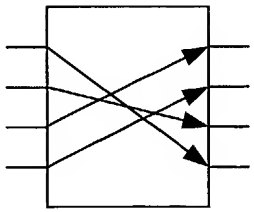


FIG. 37L

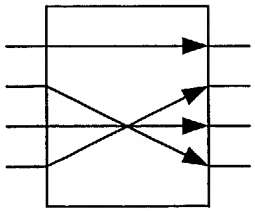


FIG. 37M

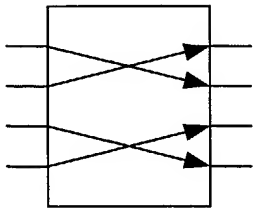


FIG. 37N

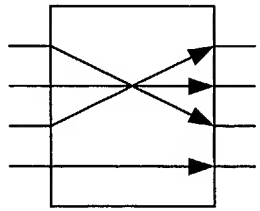


FIG. 37O

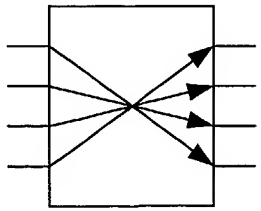
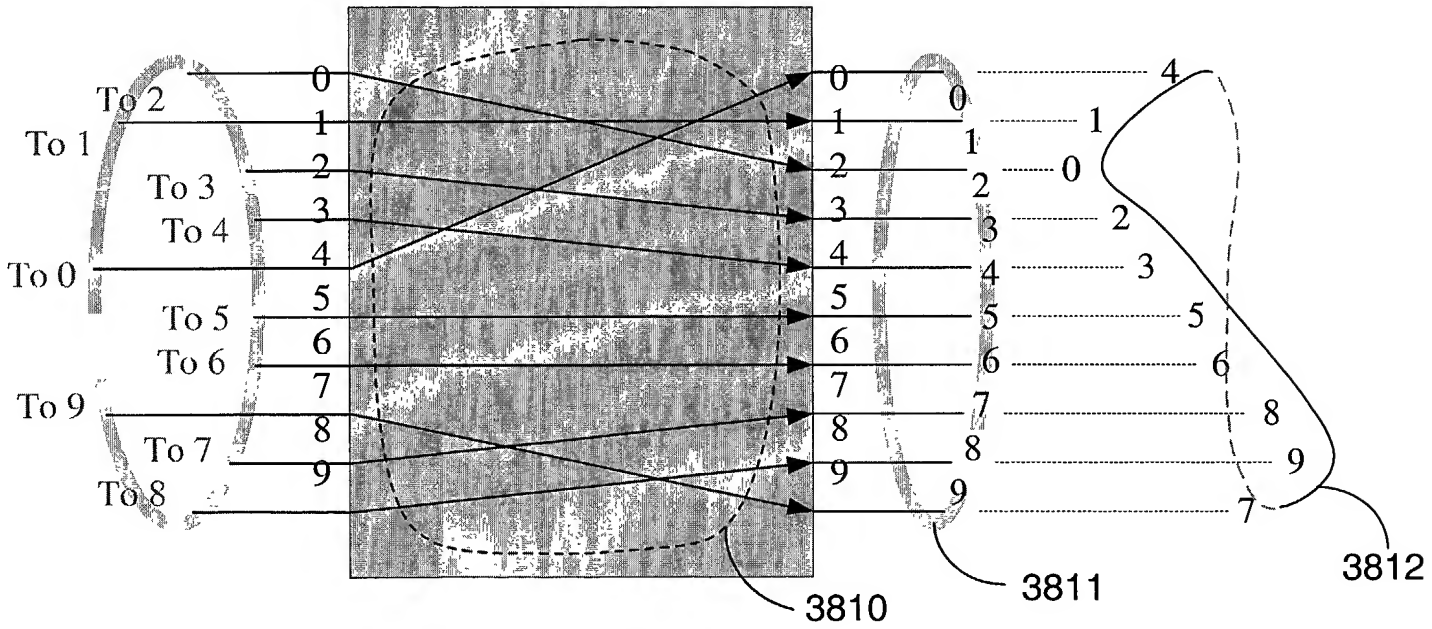


FIG. 37P


To 2
To 1
To 3
To 4
To 0
To 5
To 6
To 9
To 7
To 8
0
1
2
3
4
5
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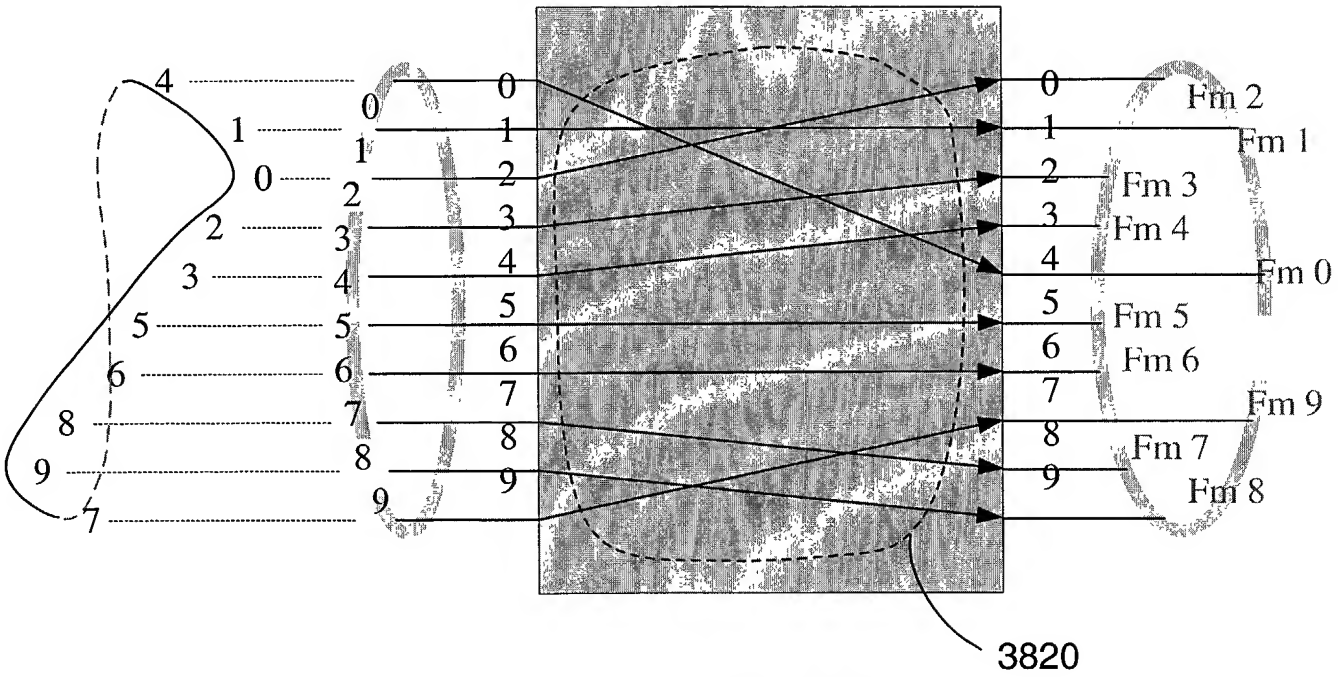
3812

FIG. 38A


4
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1
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0
1
2
3
4
5
6
7
8
9
Fm 2
Fm 1
Fm 3
Fm 4
Fm 0
Fm 5
Fm 6
Fm 9
Fm 7
Fm 8
3820

FIG.38B

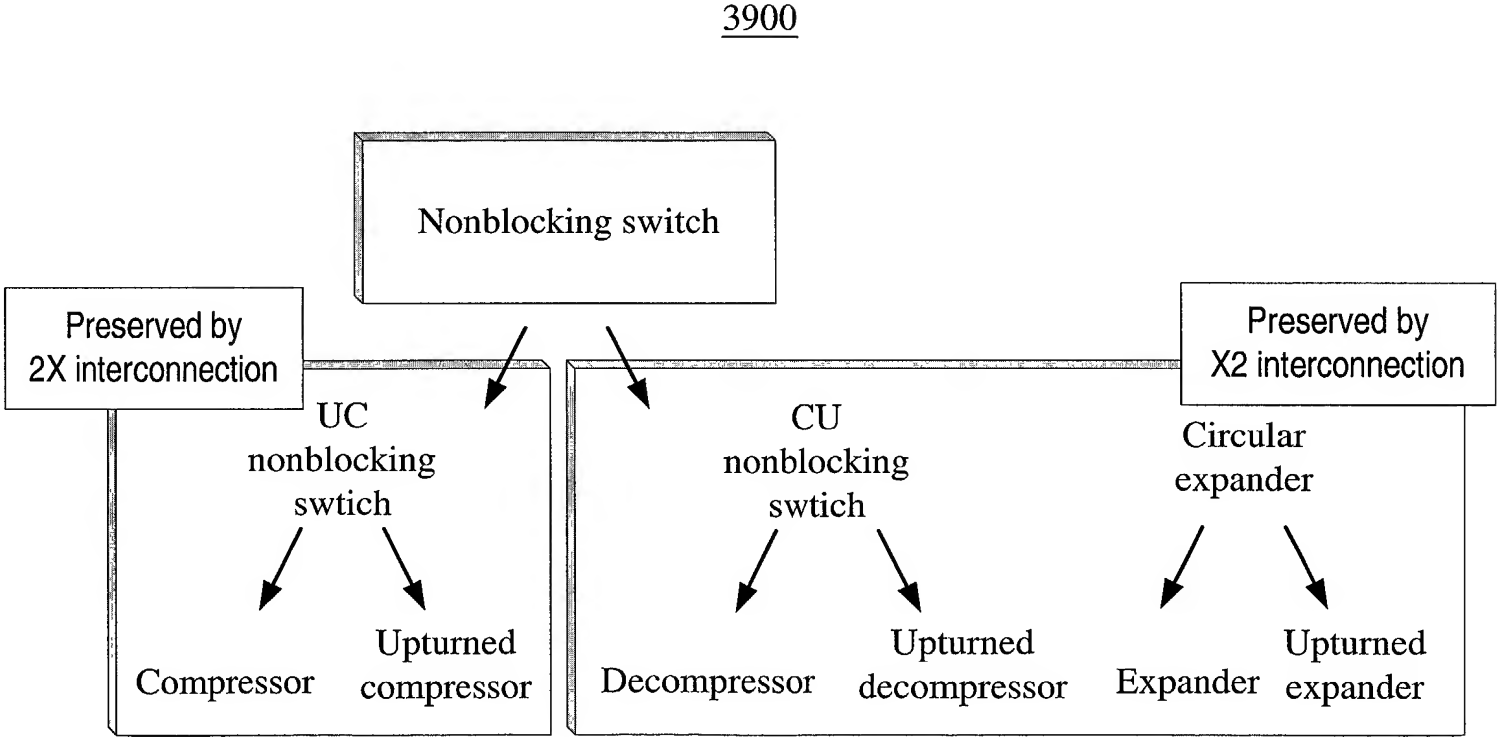
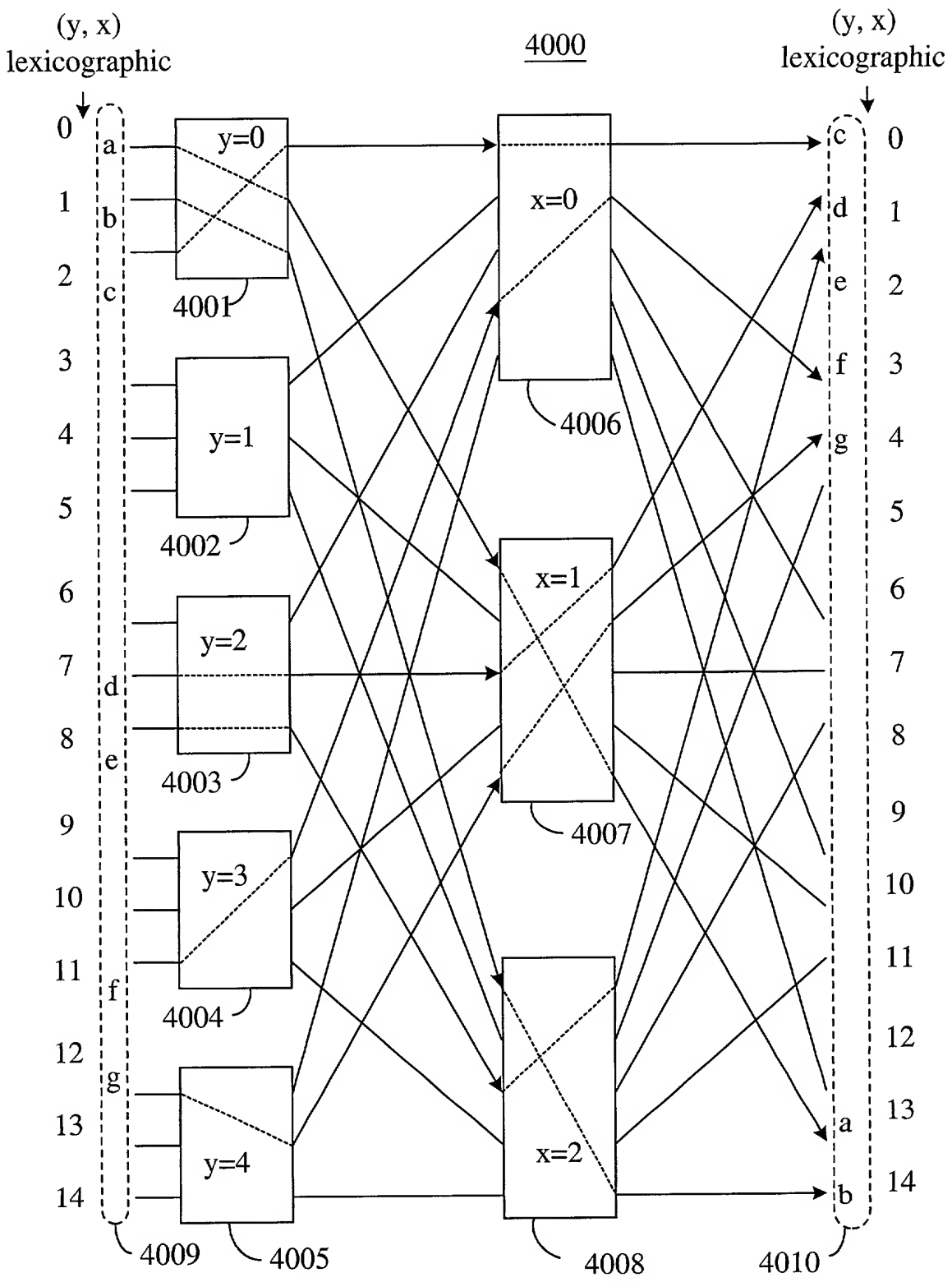

3900
Nonblocking switch
Preserved by 2X interconnection
Preserved by X2 interconnection
UC nonblocking swtich
CU nonblocking swtich
Circular expander
Compressor
Upturned compressor
Decompressor
Upturned decompressor
Expander
Upturned expander

FIG. 39


(y, x)
lexicographic
4000
(y, x)
lexicographic
0
1
2
3
4
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7
8
9
10
11
12
13
14
a
b
c
d
e
f
g
y=0
y=1
y=2
y=3
y=4
x=0
x=1
x=2
4001
4002
4003
4004
4005
4006
4007
4008
4009
4010

FIG. 40

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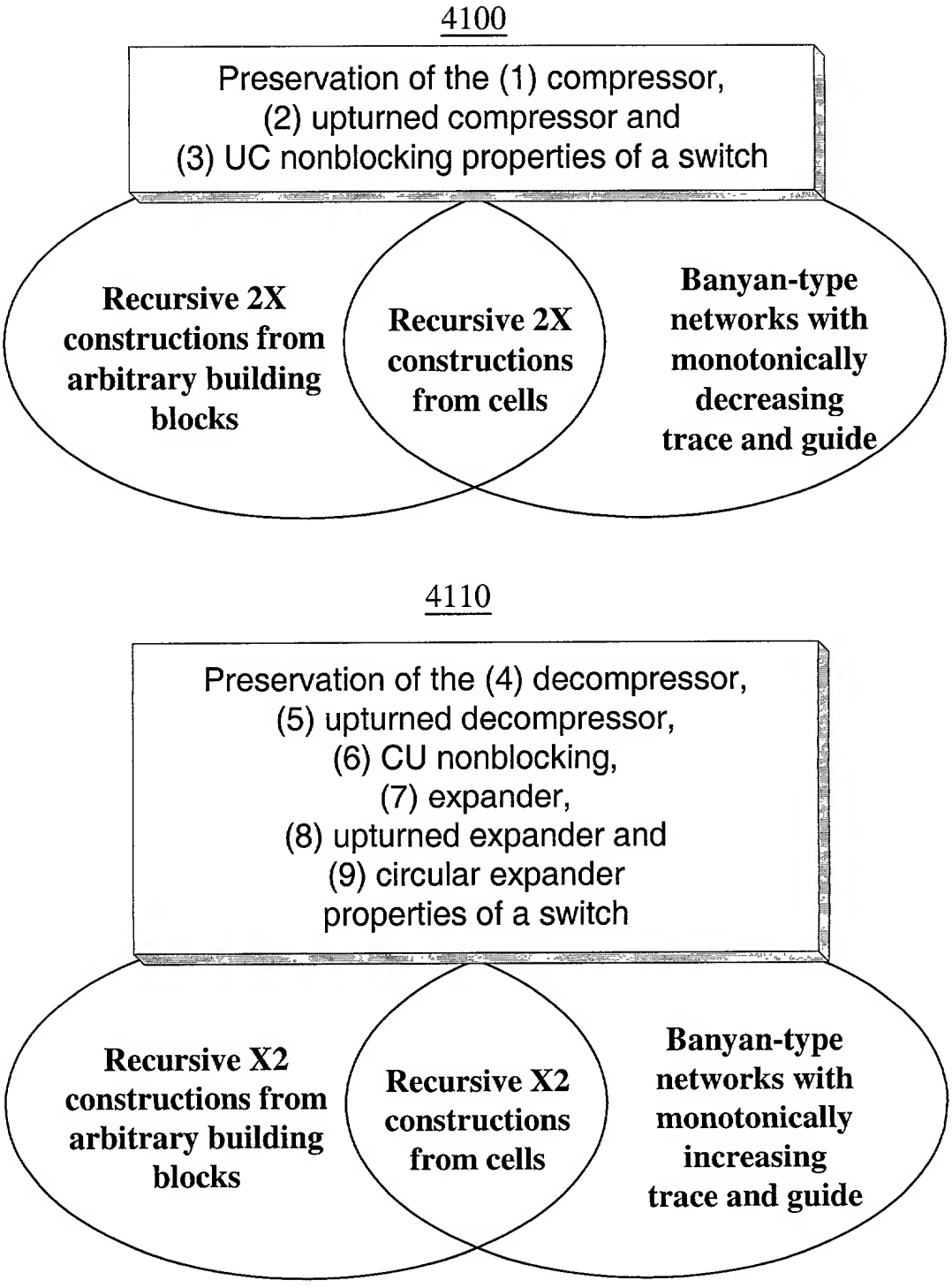

FIG. 41

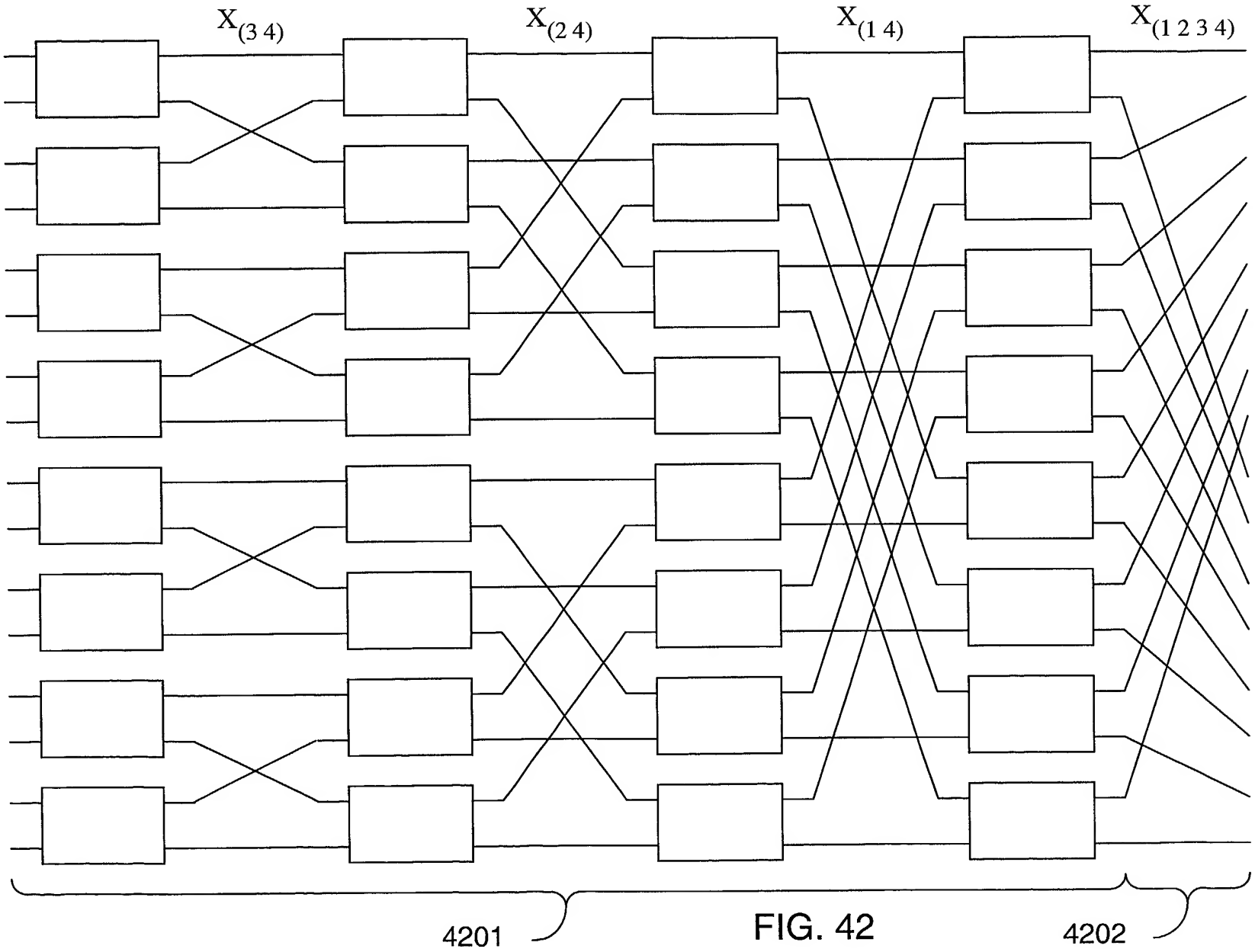

FIG. 42

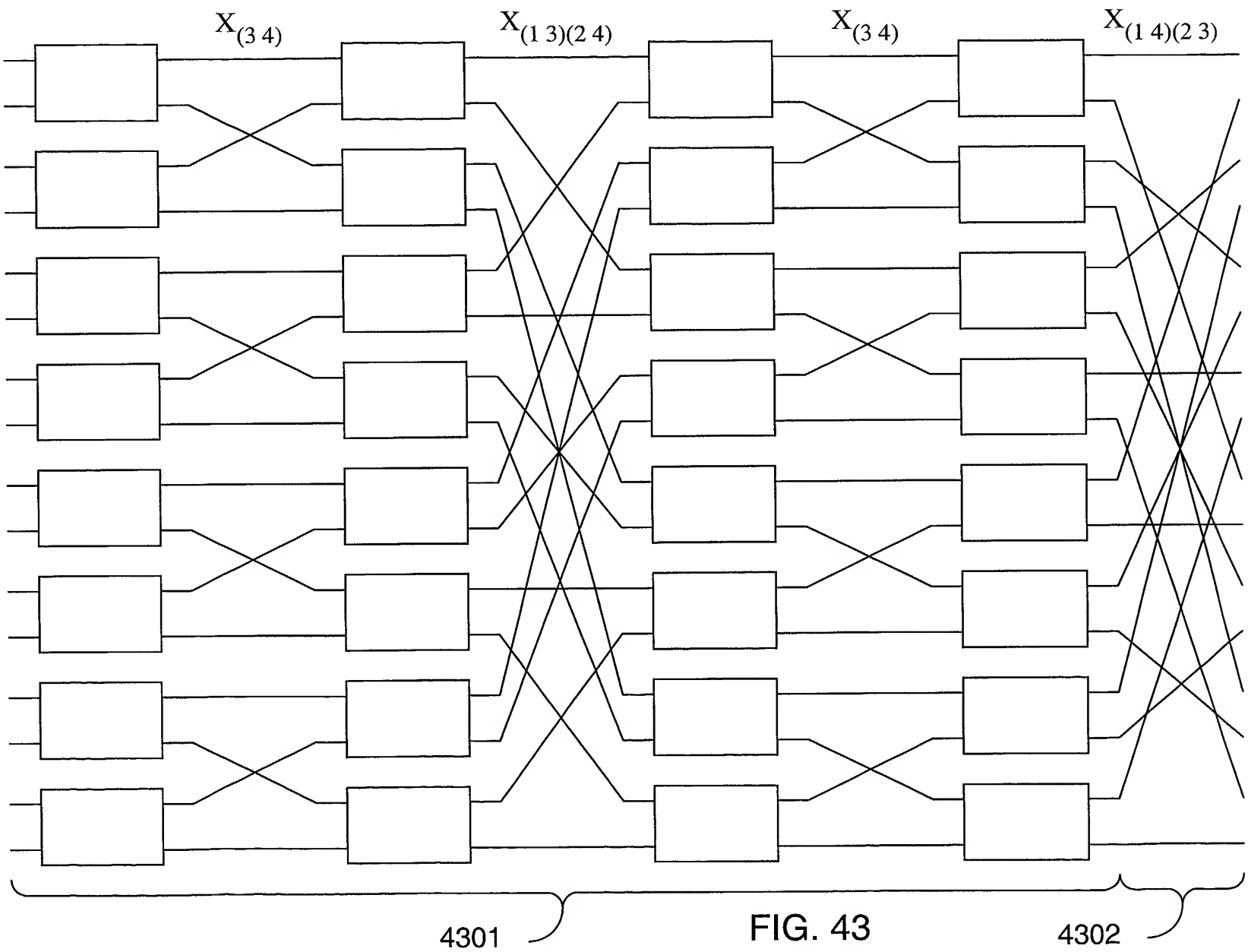

FIG. 43

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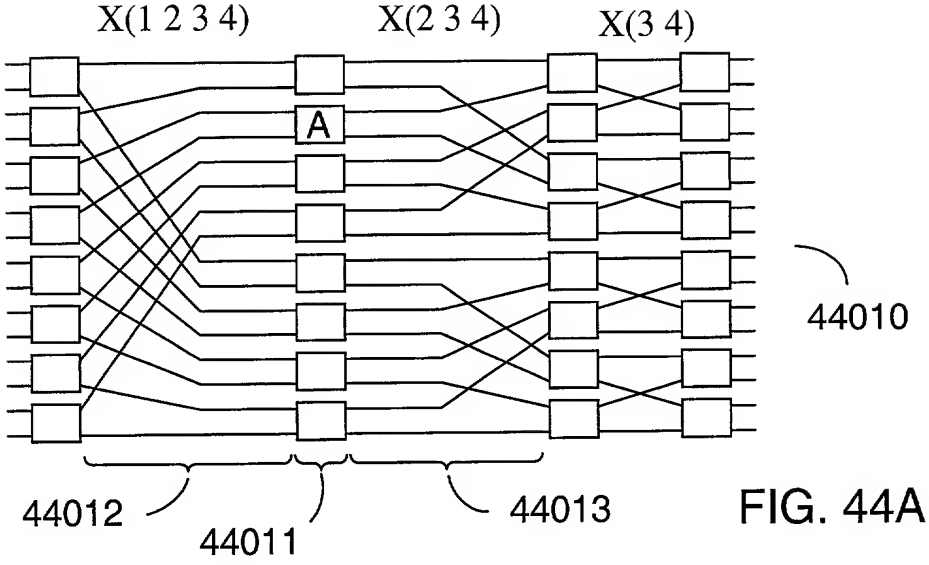

FIG. 44A

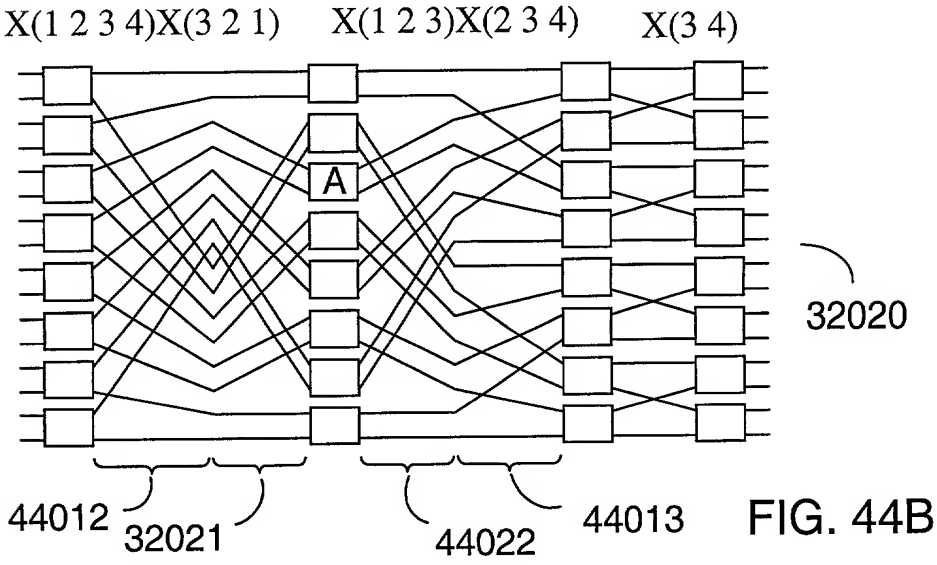

FIG. 44B

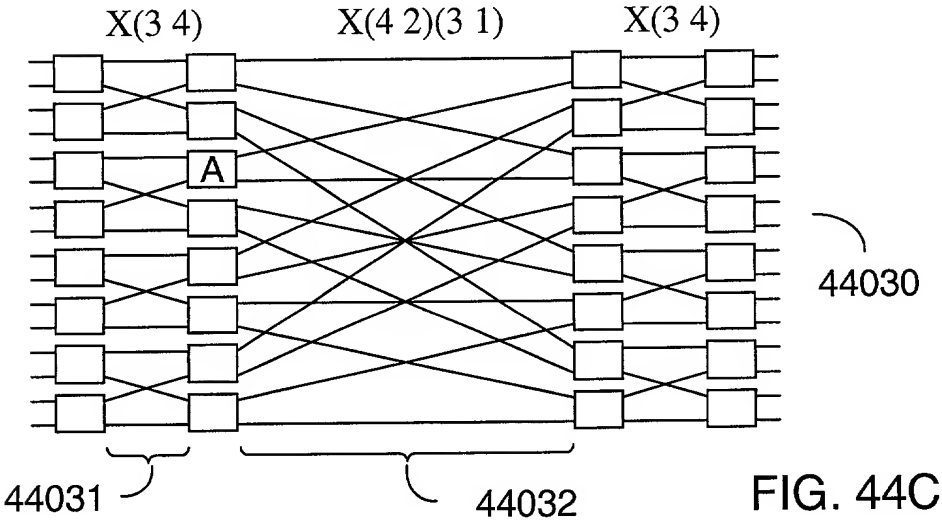

FIG. 44C

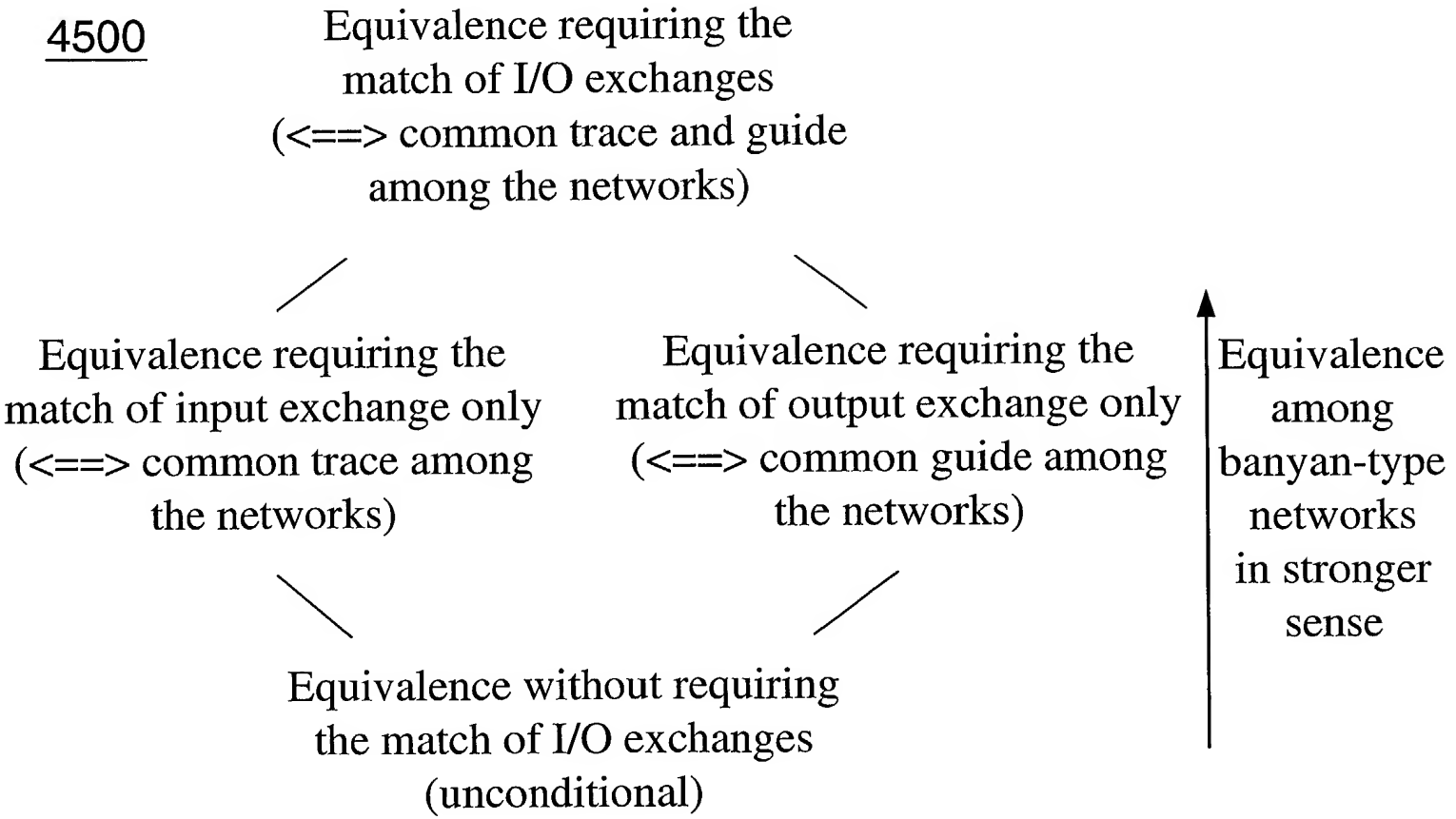
4500
Equivalence requiring the match of I/O exchanges (<==> common trace and guide among the networks)
Equivalence requiring the match of input exchange only (<==> common trace among the networks)
Equivalence requiring the match of output exchange only (<==> common guide among the networks)
Equivalence without requiring the match of I/O exchanges (unconditional)
Equivalence among banyan-type networks in stronger sense

FIG. 45

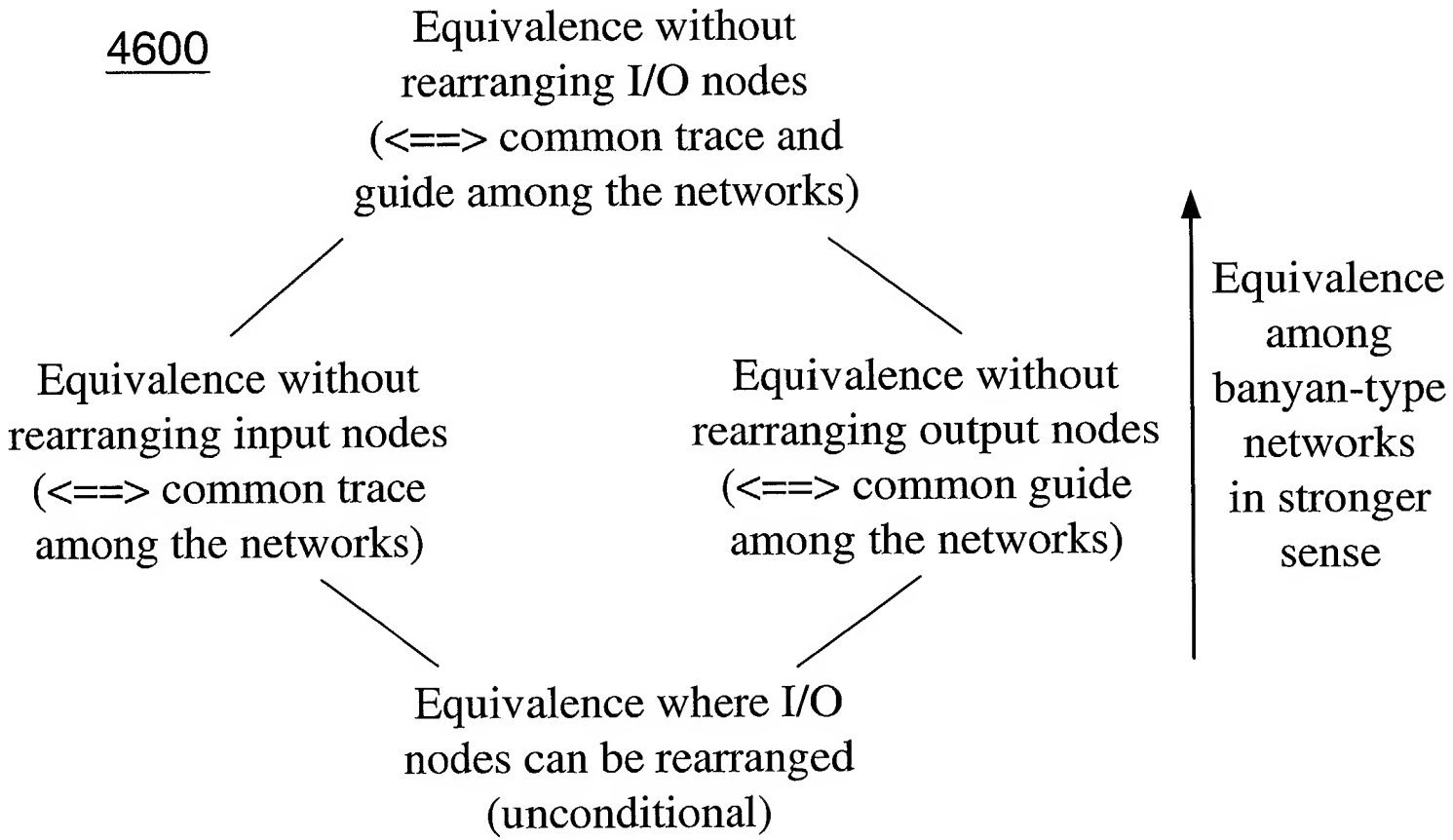
4600
Equivalence without rearranging I/O nodes (<==> common trace and guide among the networks)
Equivalence without rearranging input nodes (<==> common trace among the networks)
Equivalence without rearranging output nodes (<==> common guide among the networks)
Equivalence where I/O nodes can be rearranged (unconditional)
Equivalence among banyan-type networks in stronger sense

FIG. 46

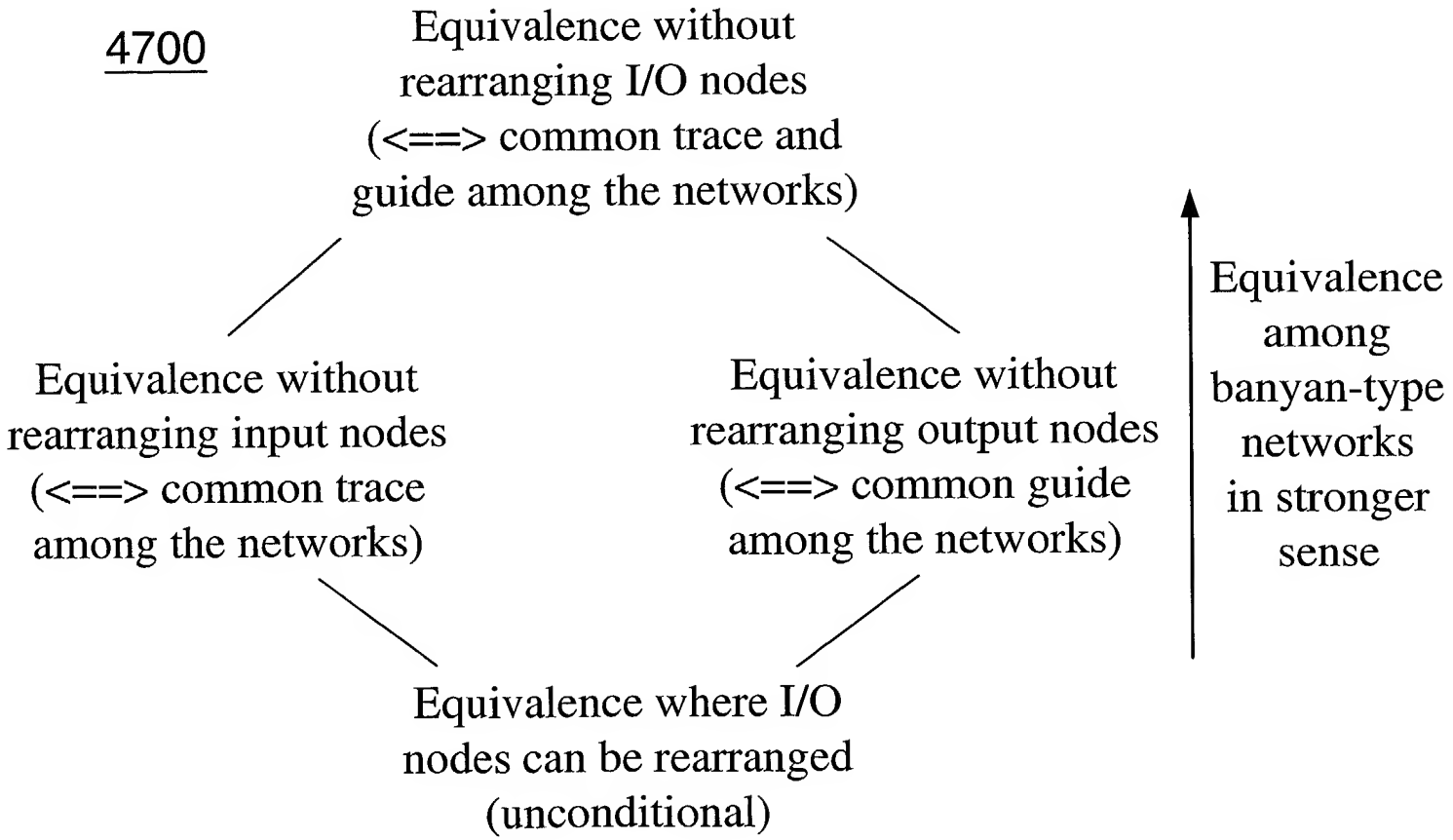
4700
Equivalence without rearranging I/O nodes (<==> common trace and guide among the networks)
Equivalence without rearranging input nodes (<==> common trace among the networks)
Equivalence without rearranging output nodes (<==> common guide among the networks)
Equivalence where I/O nodes can be rearranged (unconditional)
Equivalence among banyan-type networks in stronger sense

FIG. 47

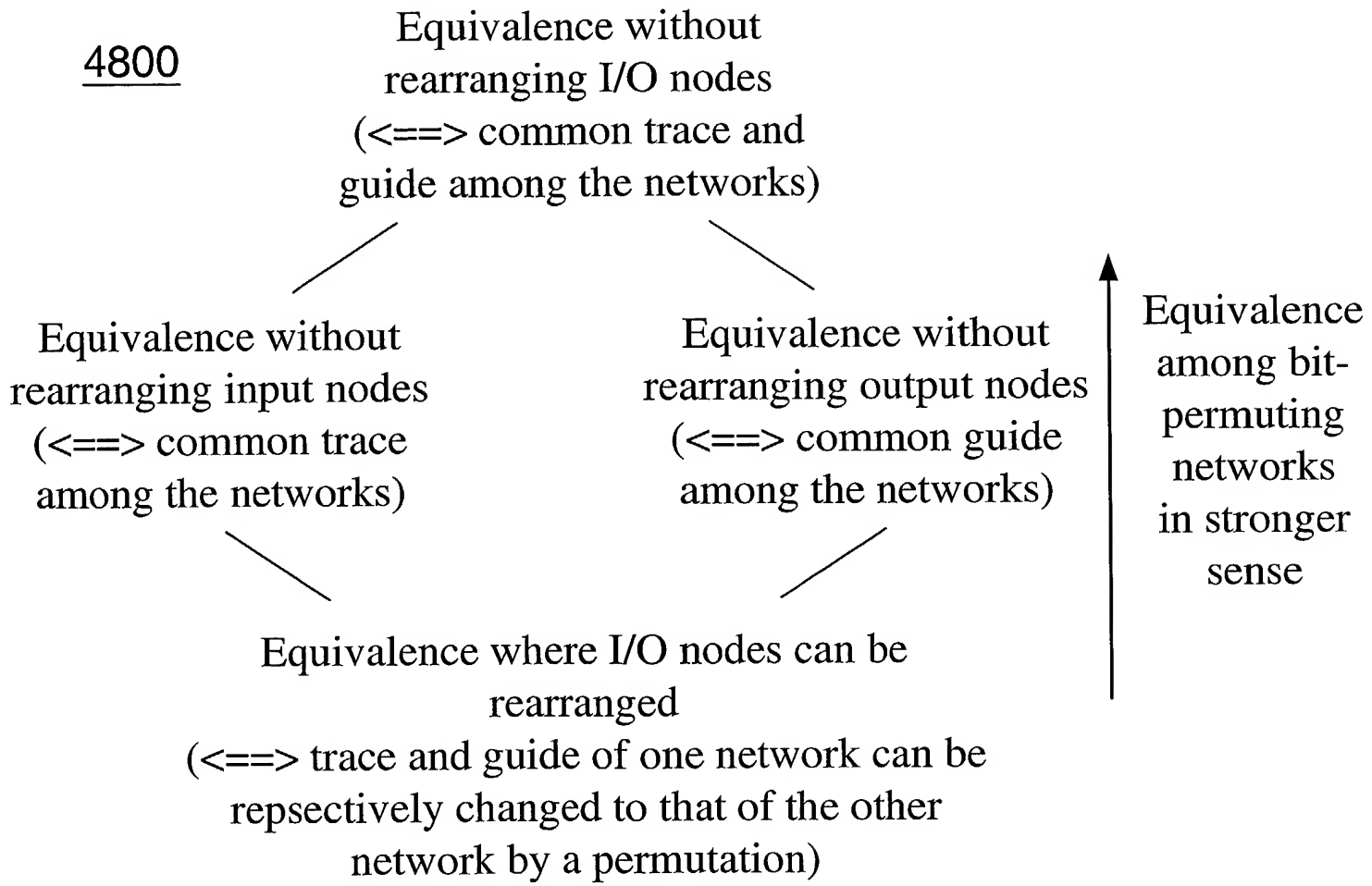
4800
Equivalence without rearranging I/O nodes (<==> common trace and guide among the networks)
Equivalence without rearranging input nodes (<==> common trace among the networks)
Equivalence without rearranging output nodes (<==> common guide among the networks)
Equivalence among bit-permuting networks in stronger sense
Equivalence where I/O nodes can be rearranged (<==> trace and guide of one network can be repsectively changed to that of the other network by a permutation)

FIG. 48

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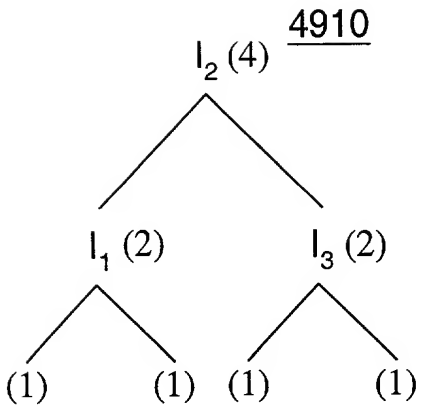

FIG. 49A

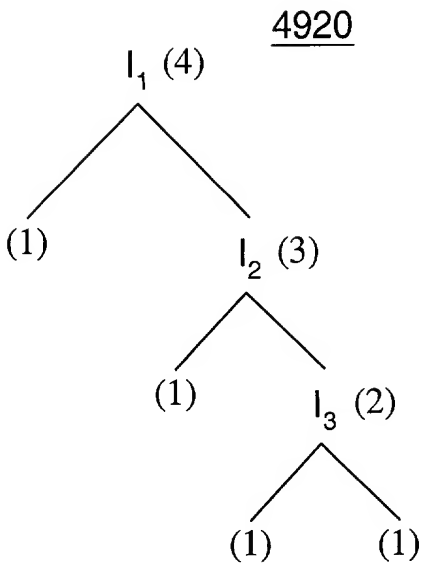

FIG. 49B

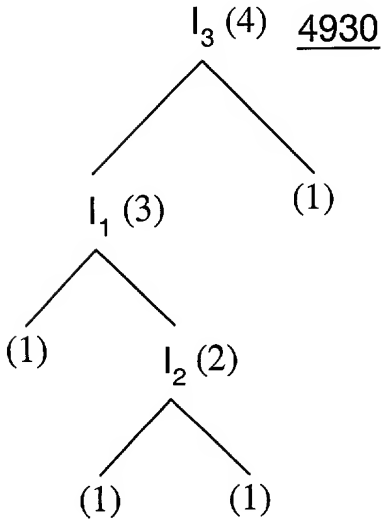

FIG. 49C

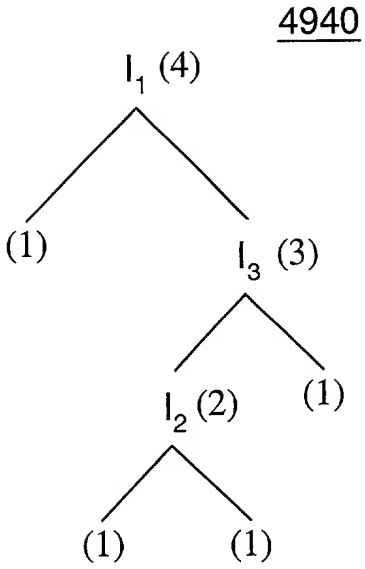

FIG. 49D

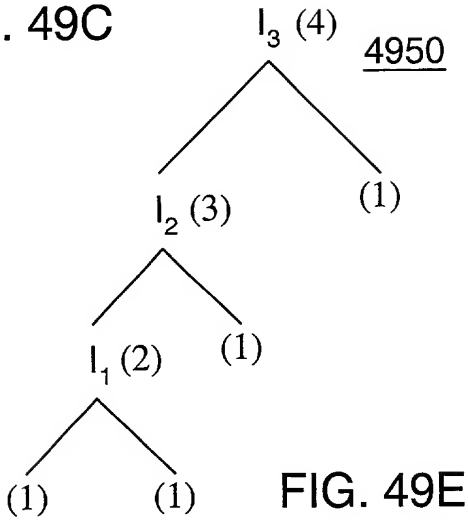

FIG. 49E

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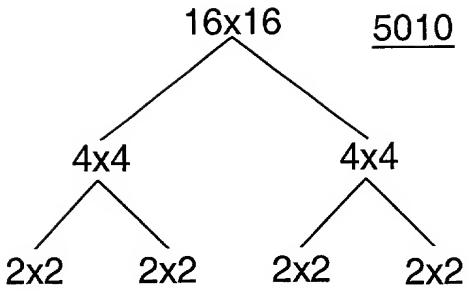

FIG. 50A

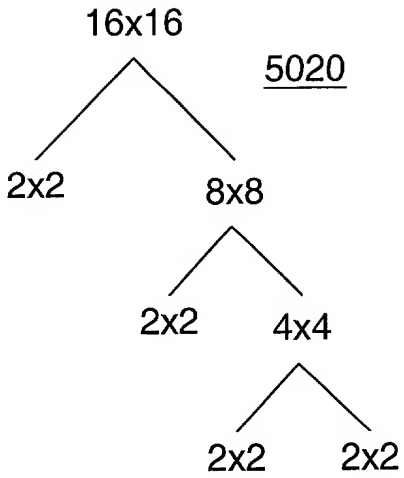

FIG. 50B

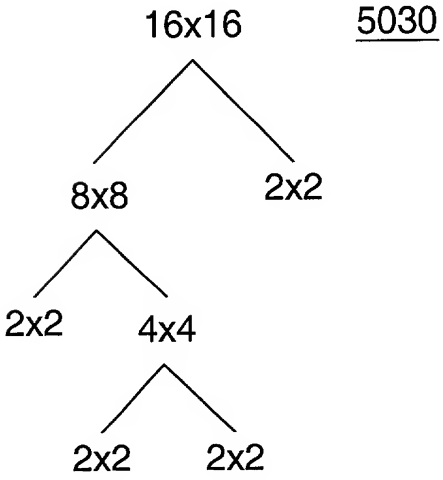

FIG. 50C

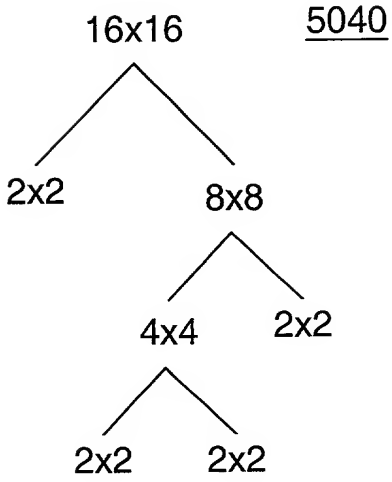

FIG. 50D

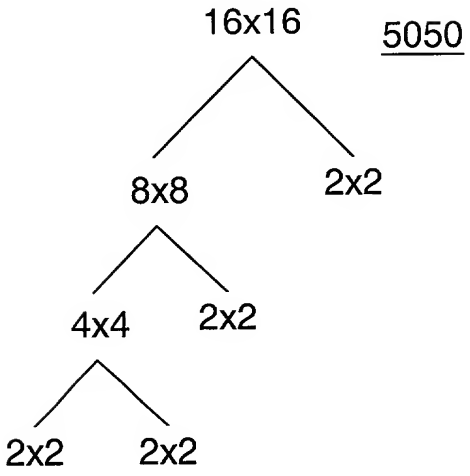

FIG. 50E

5100

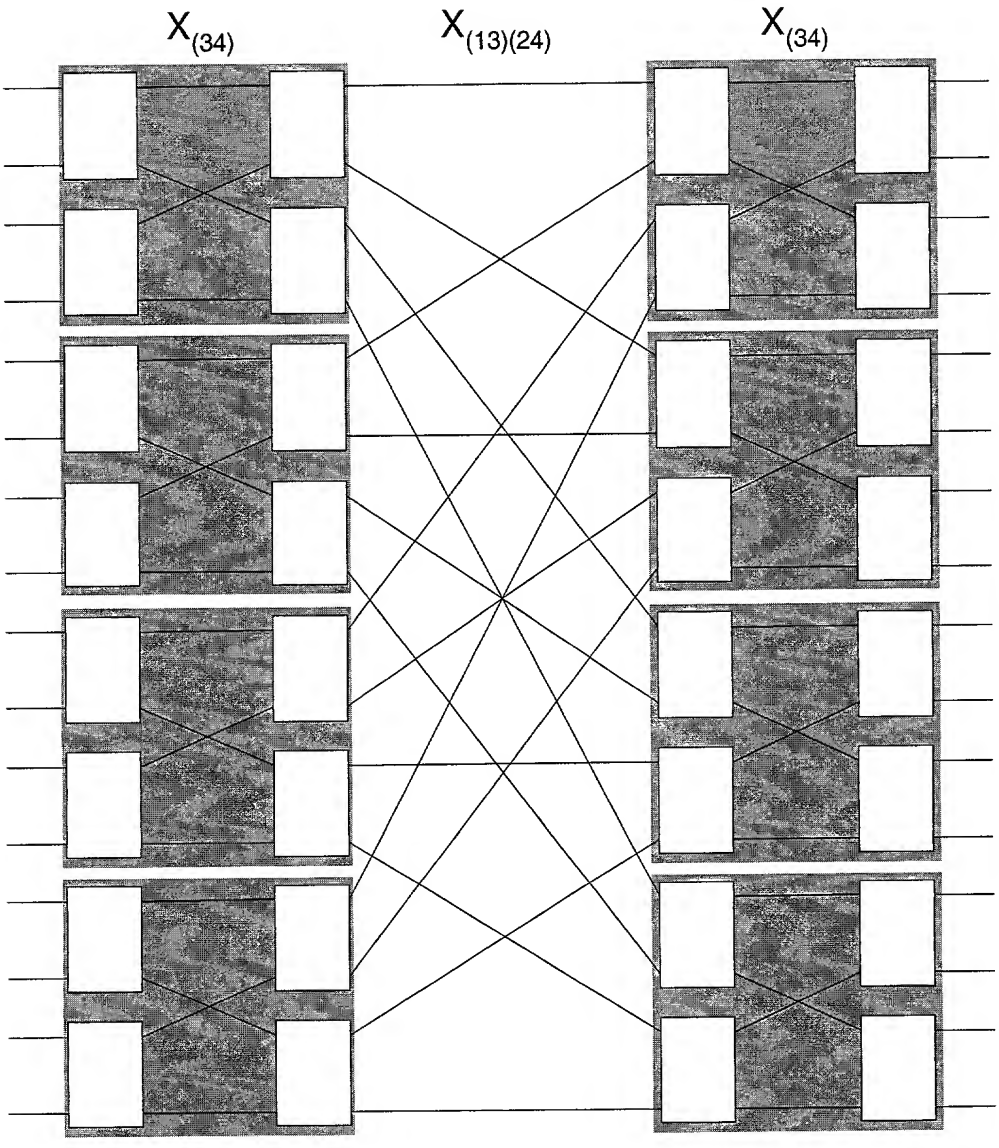

FIG. 51

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5200

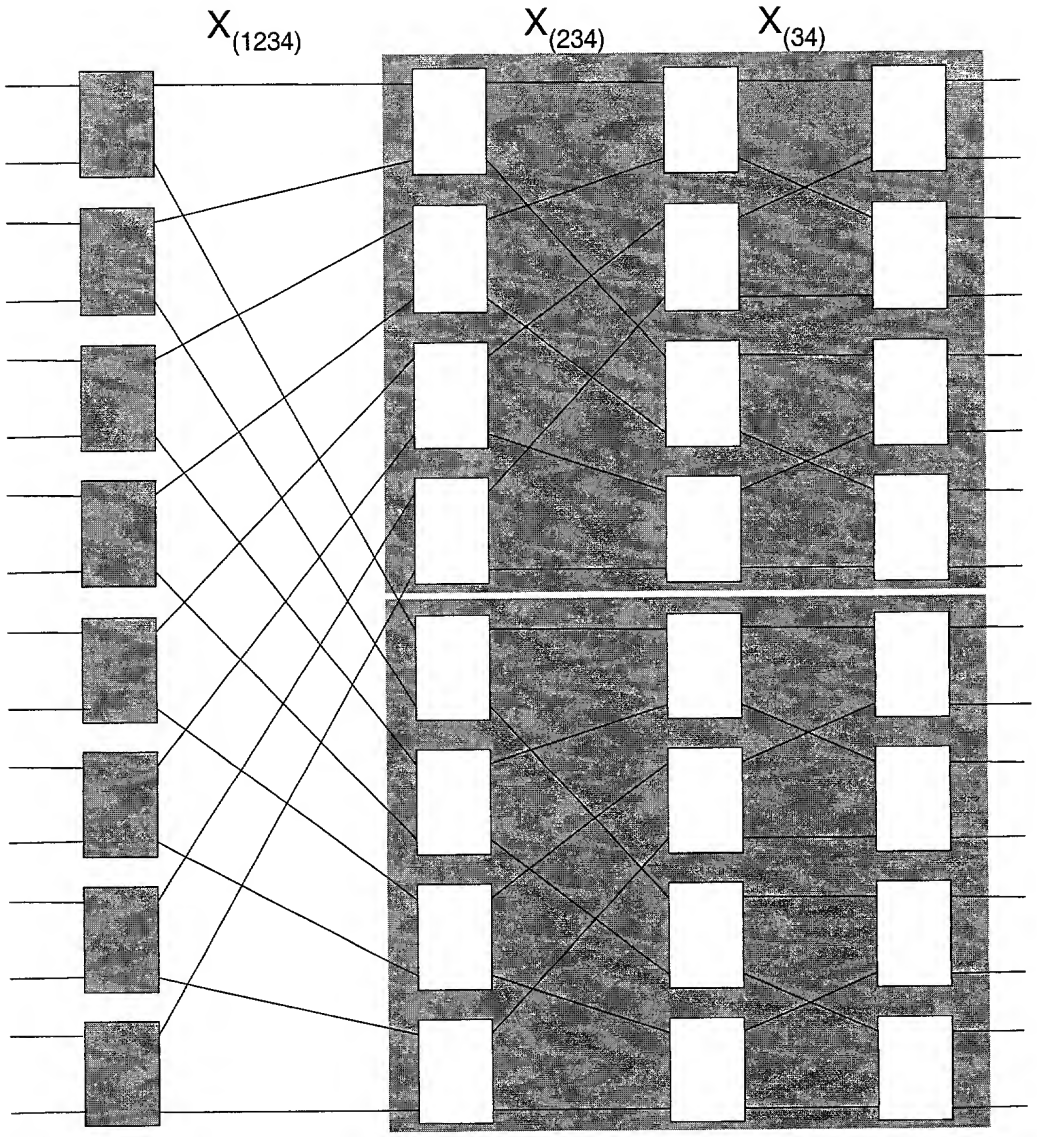
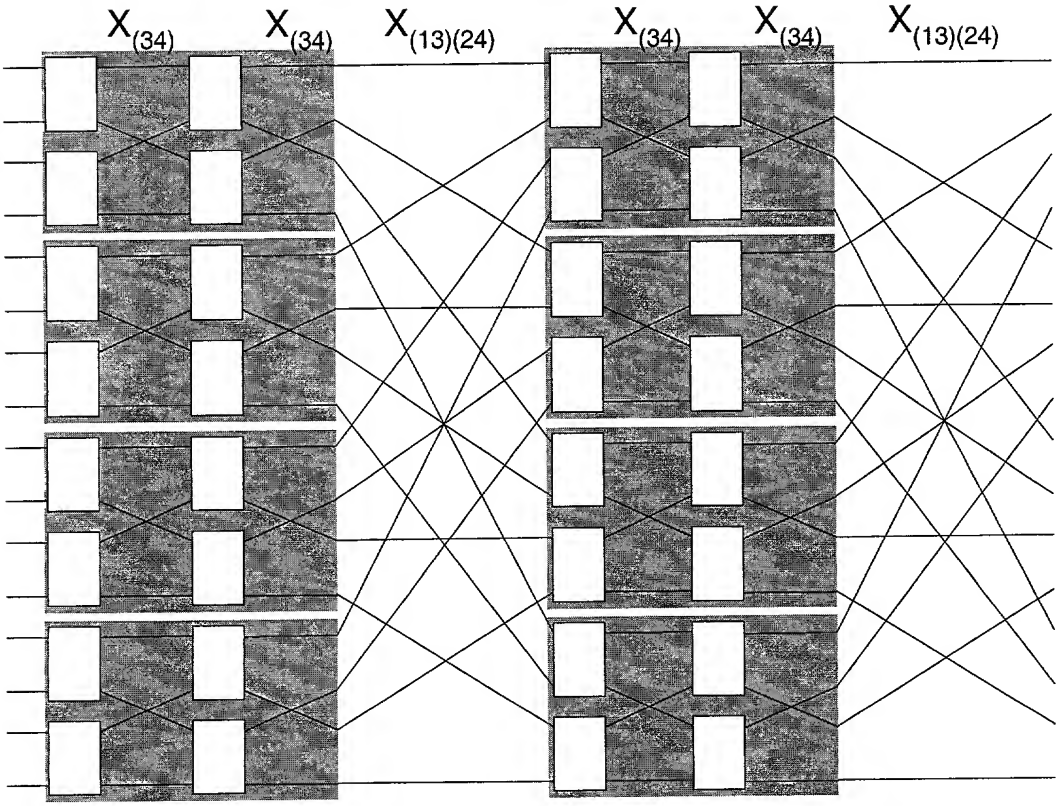
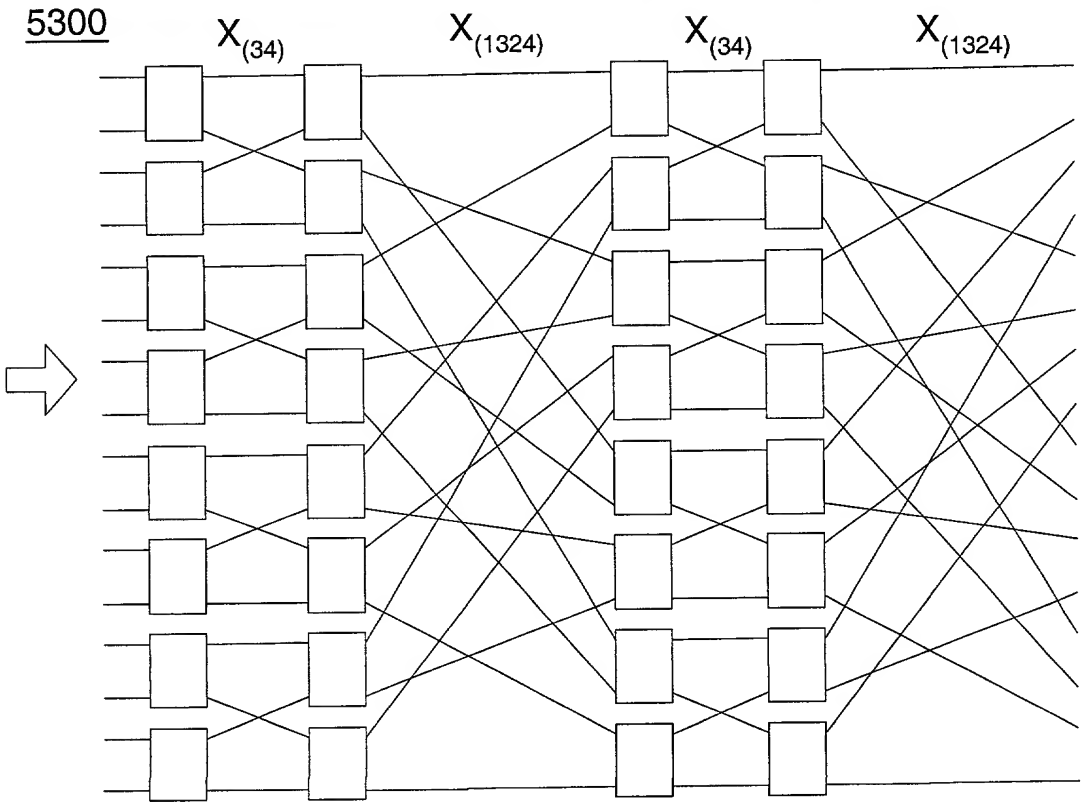


FIG. 52

FIG. 53





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5400

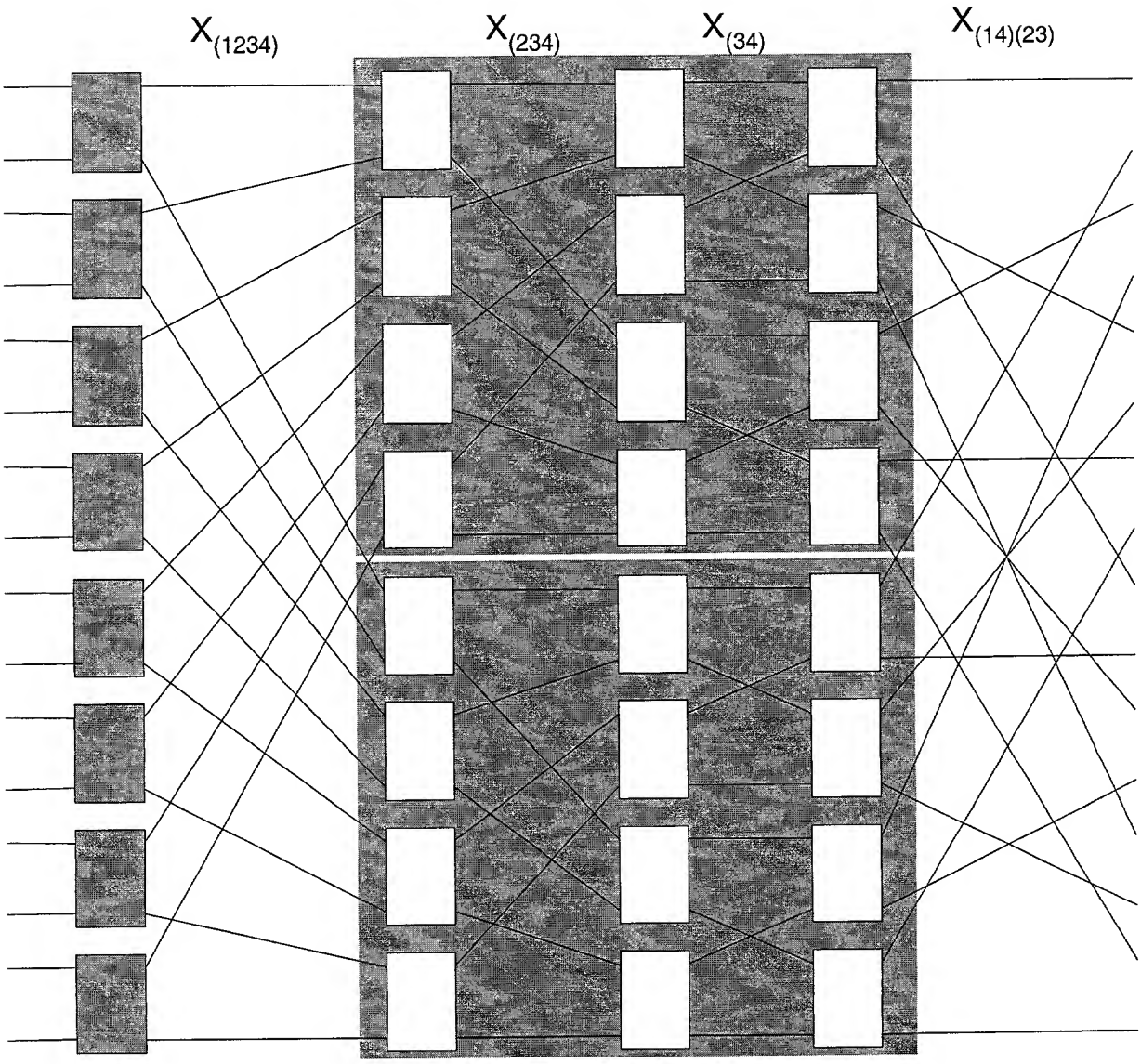

FIG. 54

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5500

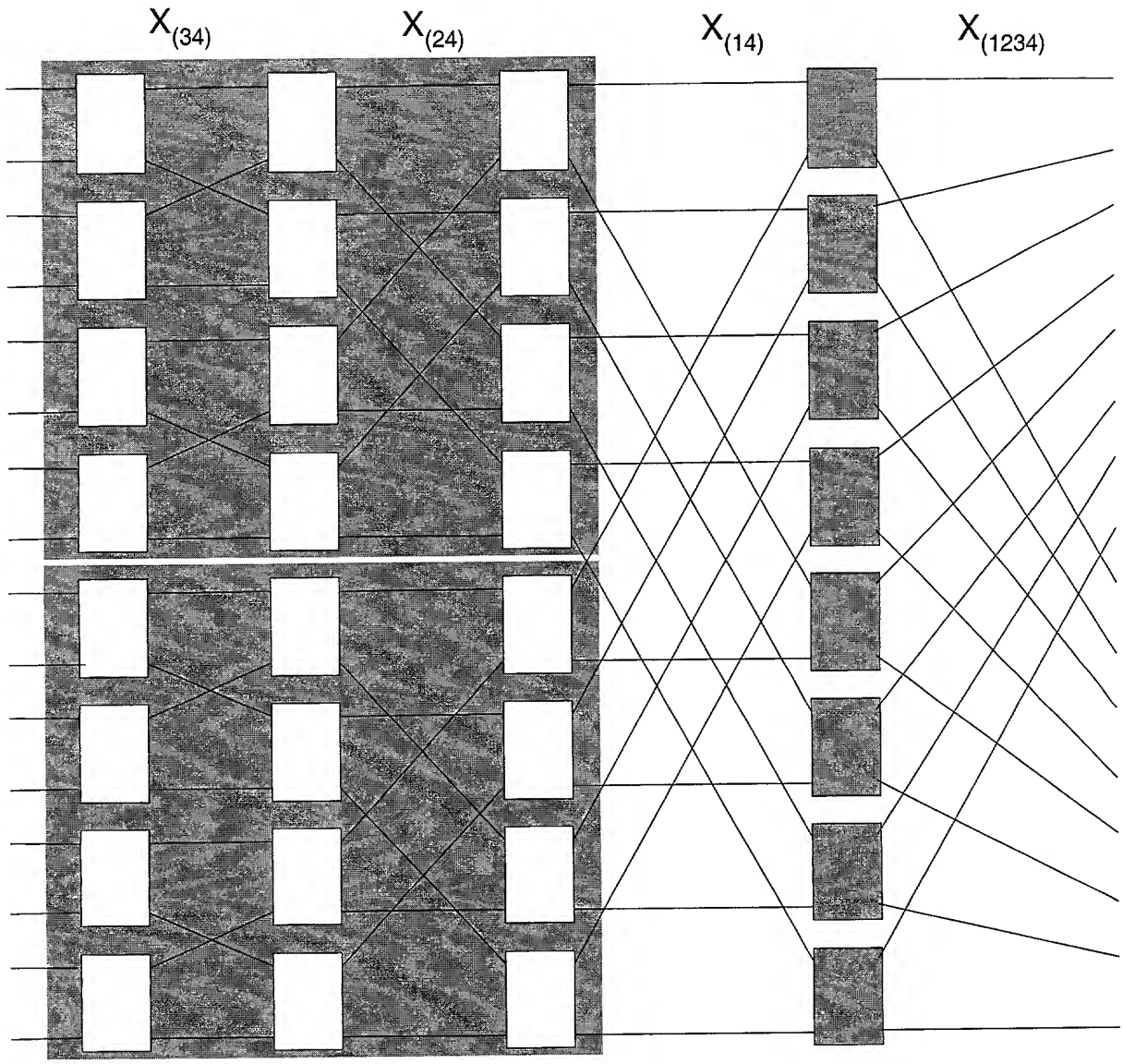


FIG. 55

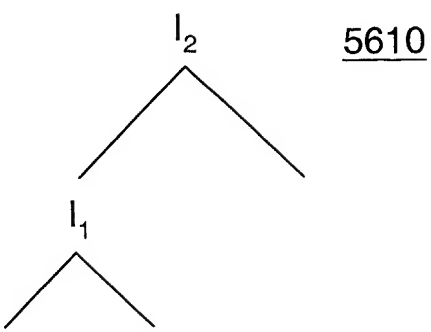


FIG. 56A

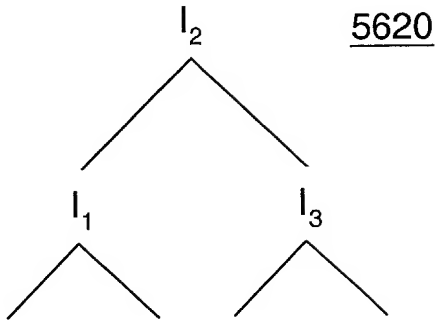


FIG. 56B

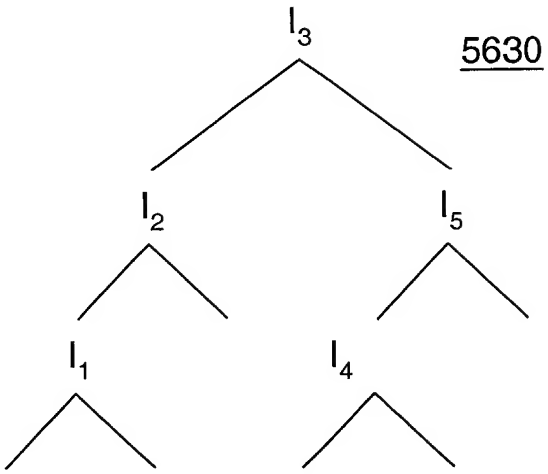


FIG. 56C

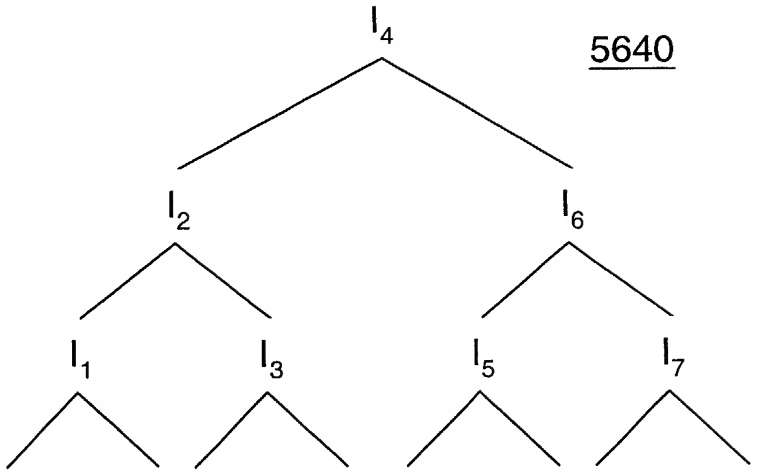


FIG. 56D

FIG. 57

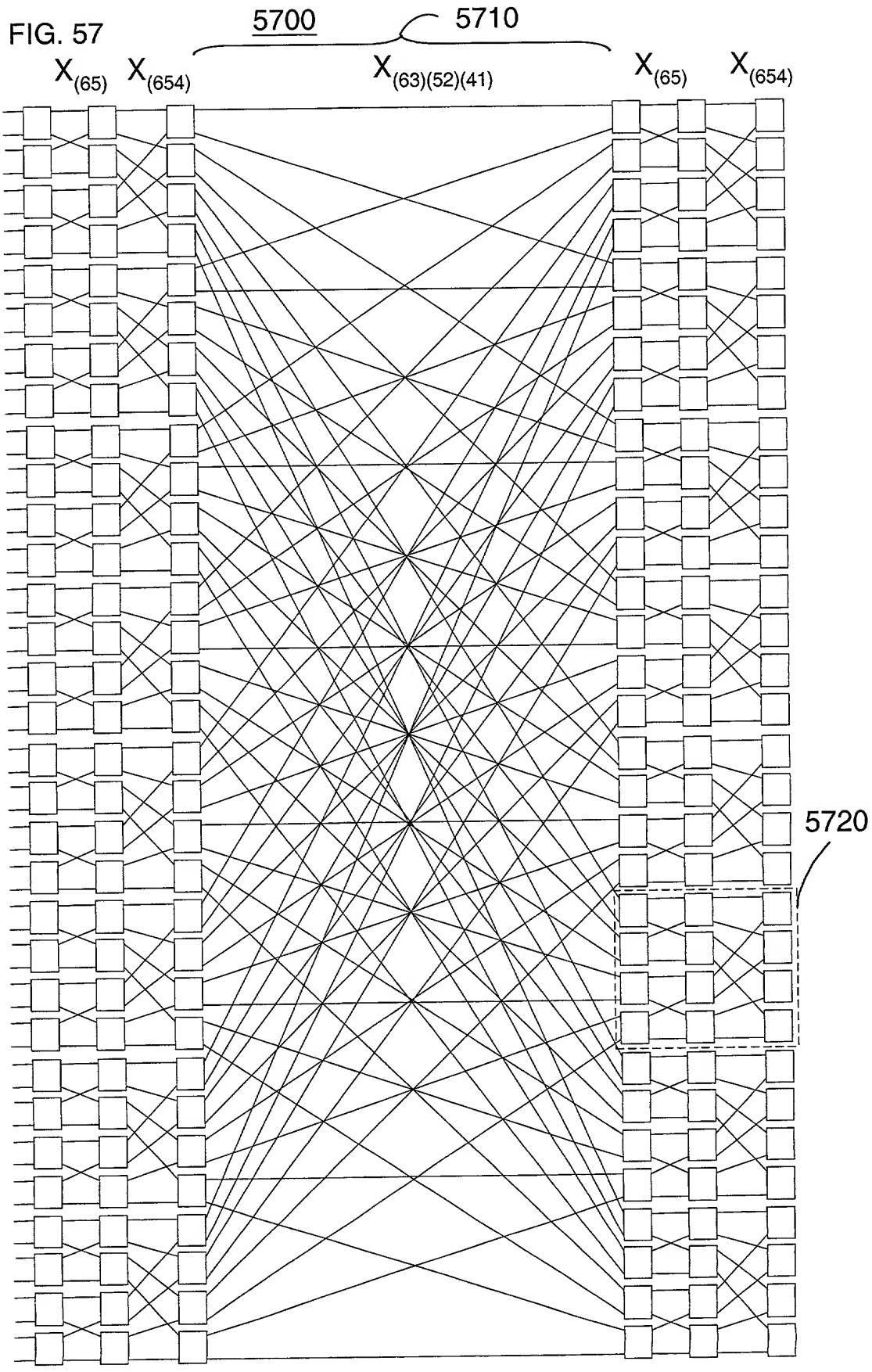


FIG. 58

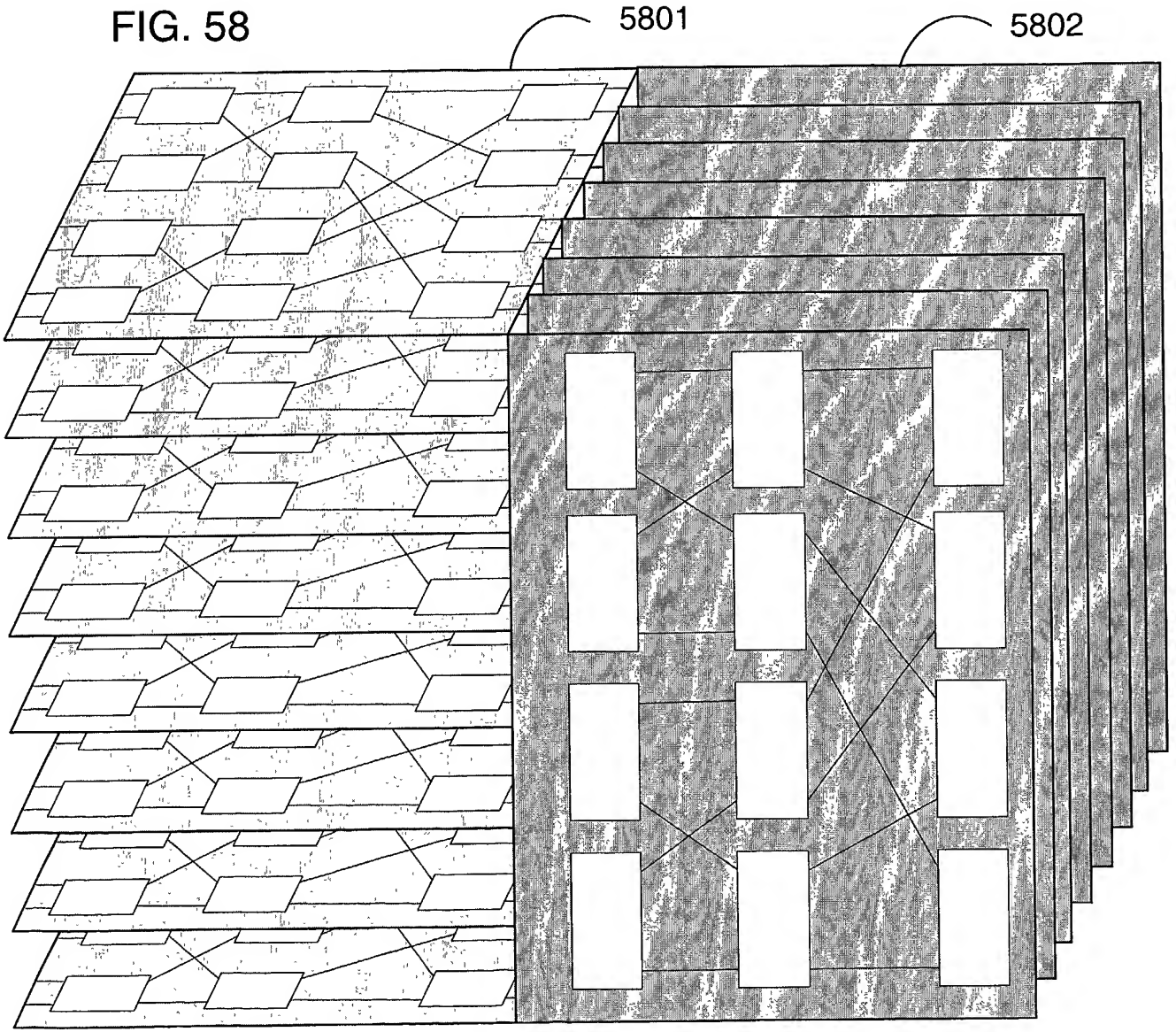
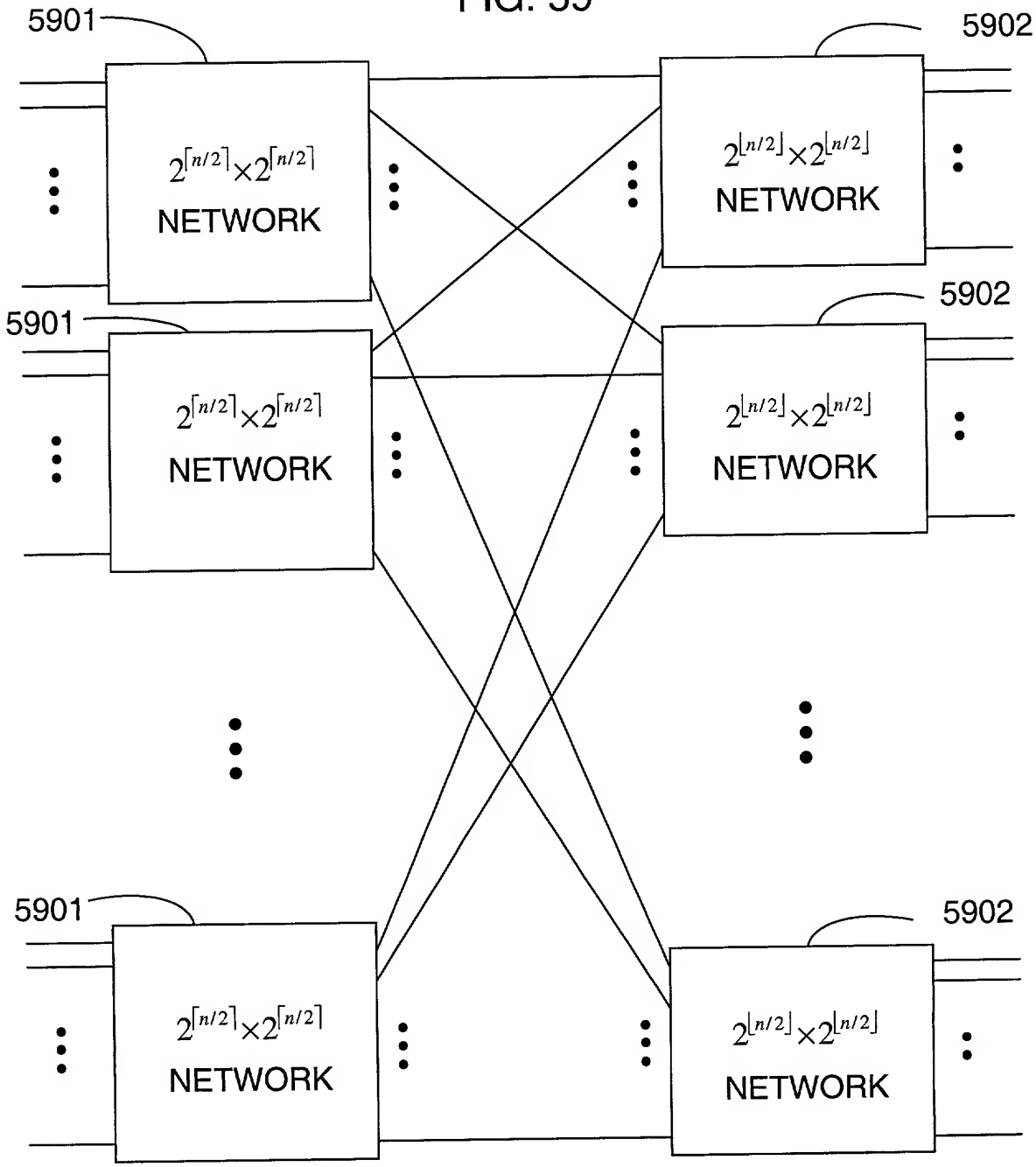


FIG. 59


5901
5902
$2^{\lceil n/2 \rceil} \times 2^{\lceil n/2 \rceil}$
NETWORK
$2^{\lfloor n/2 \rfloor} \times 2^{\lfloor n/2 \rfloor}$
NETWORK

Patent Application Publication

6000

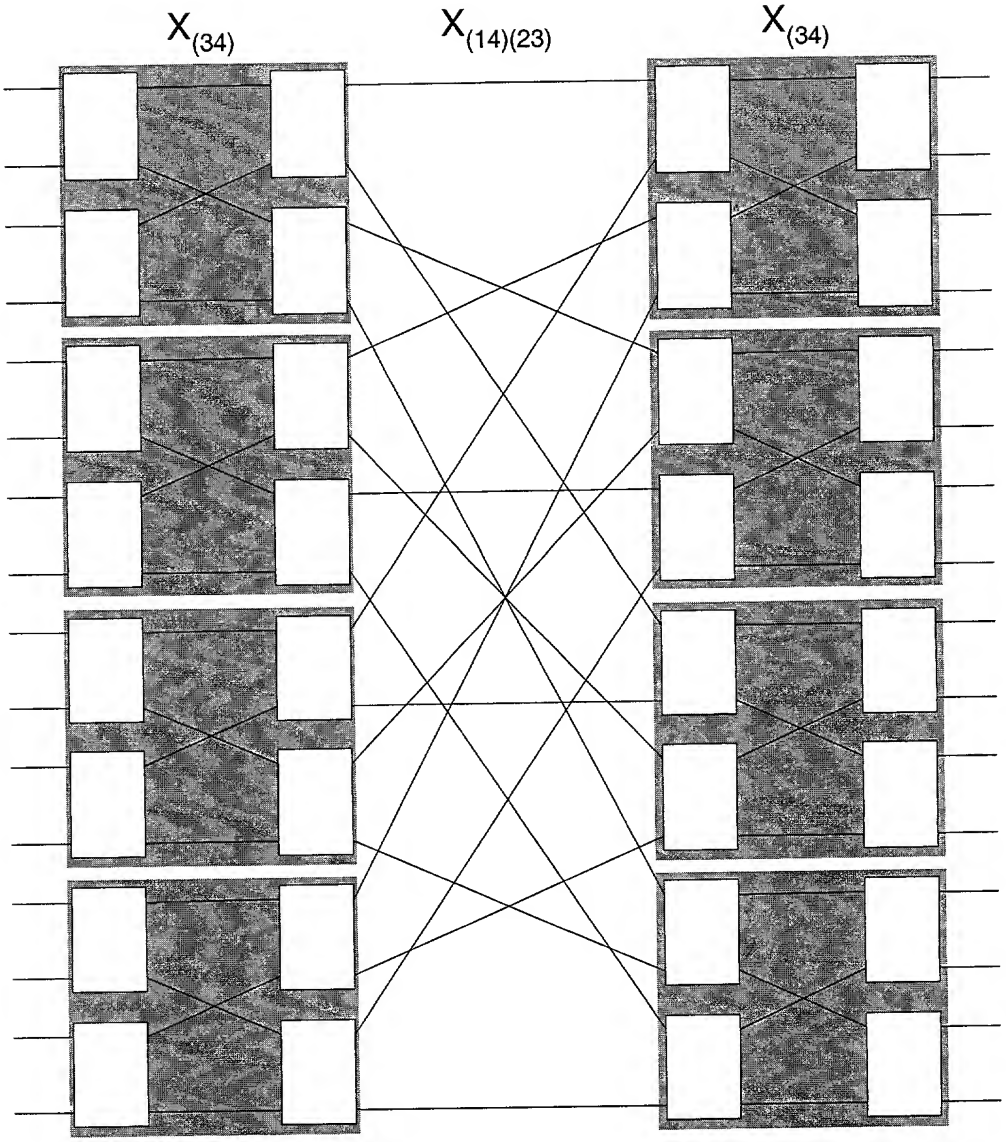
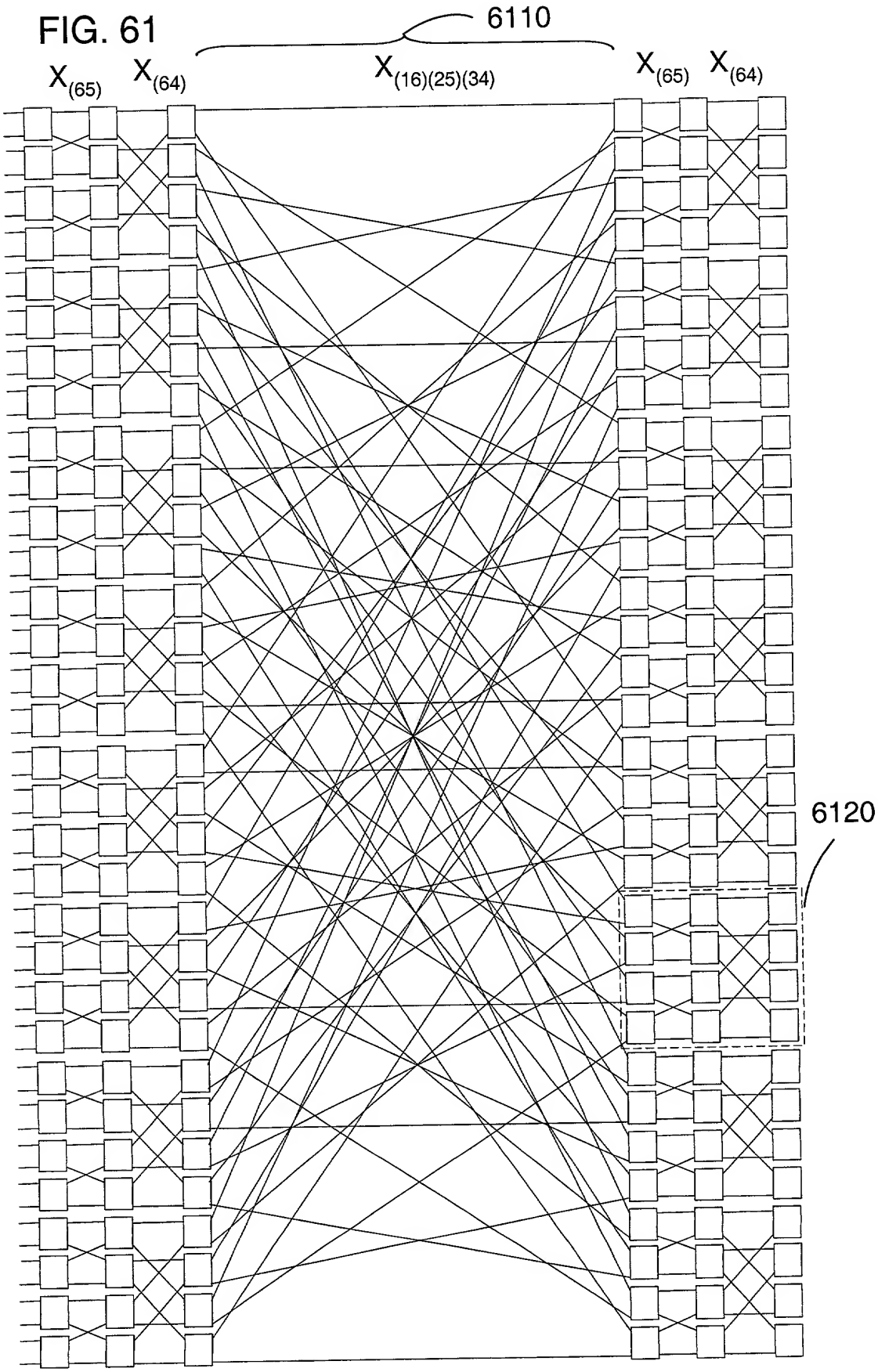


FIG. 60

FIG. 61



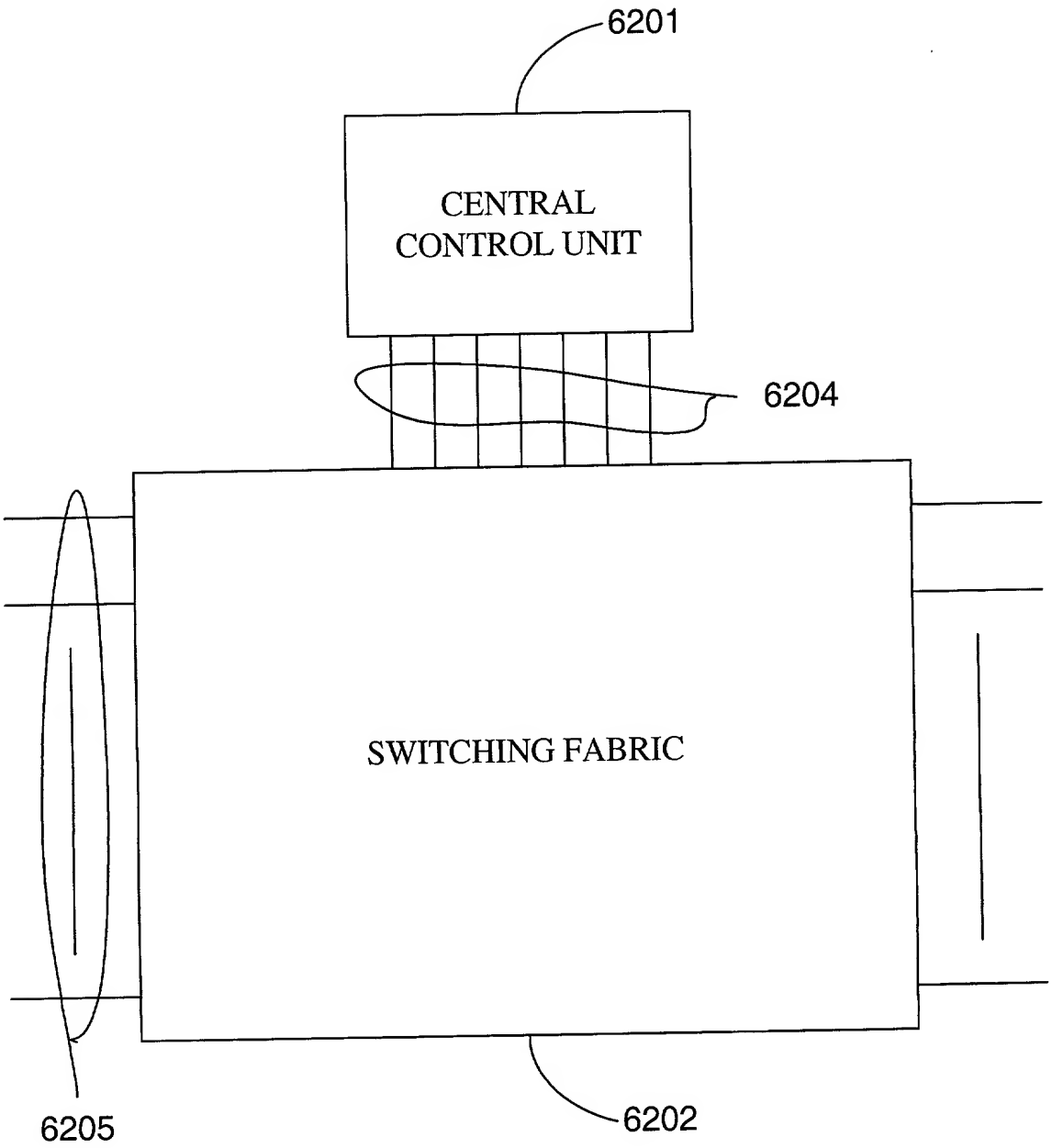


FIG. 62A

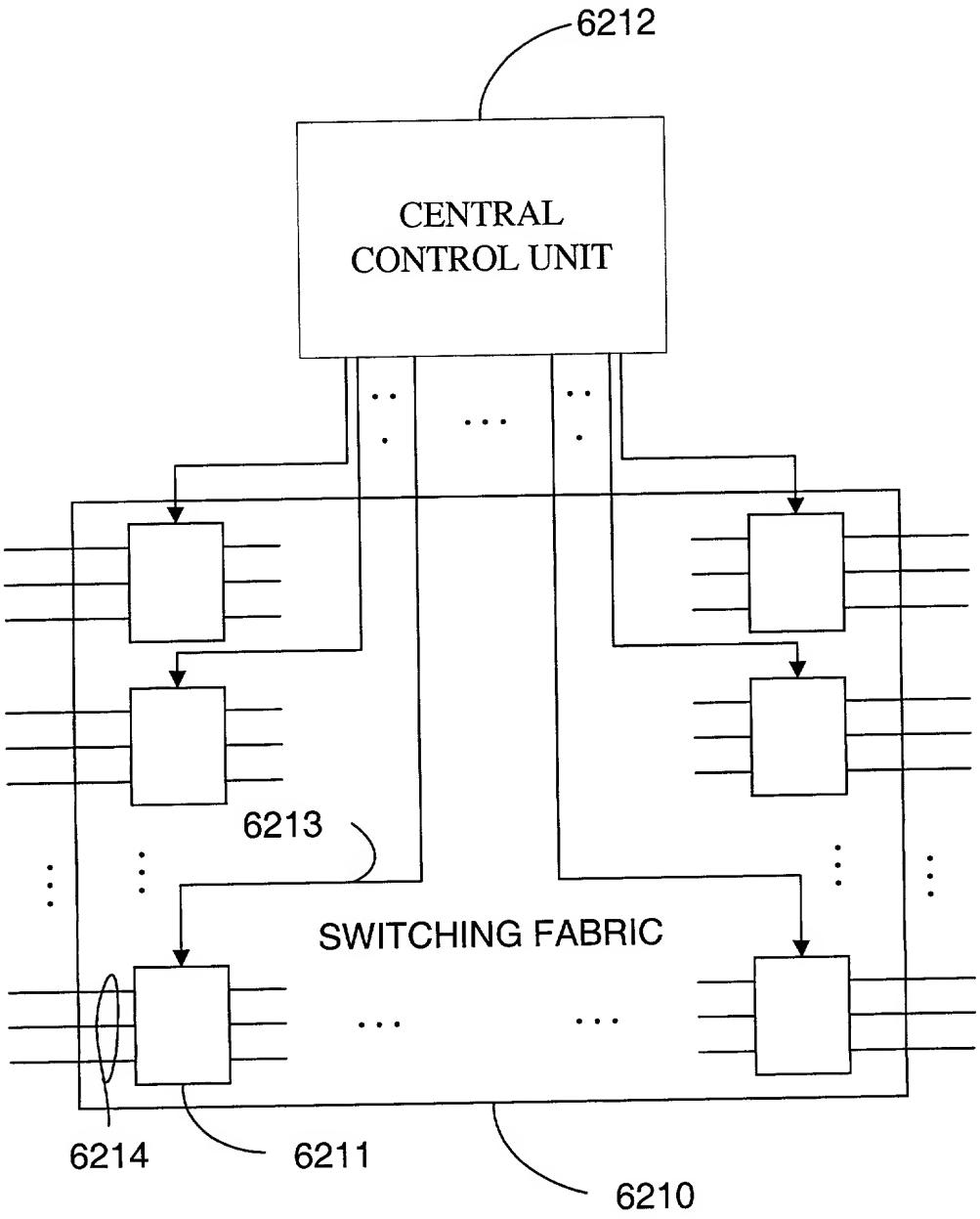

6212
CENTRAL
CONTROL UNIT
6213
SWITCHING FABRIC
6214
6211
6210

FIG. 62B

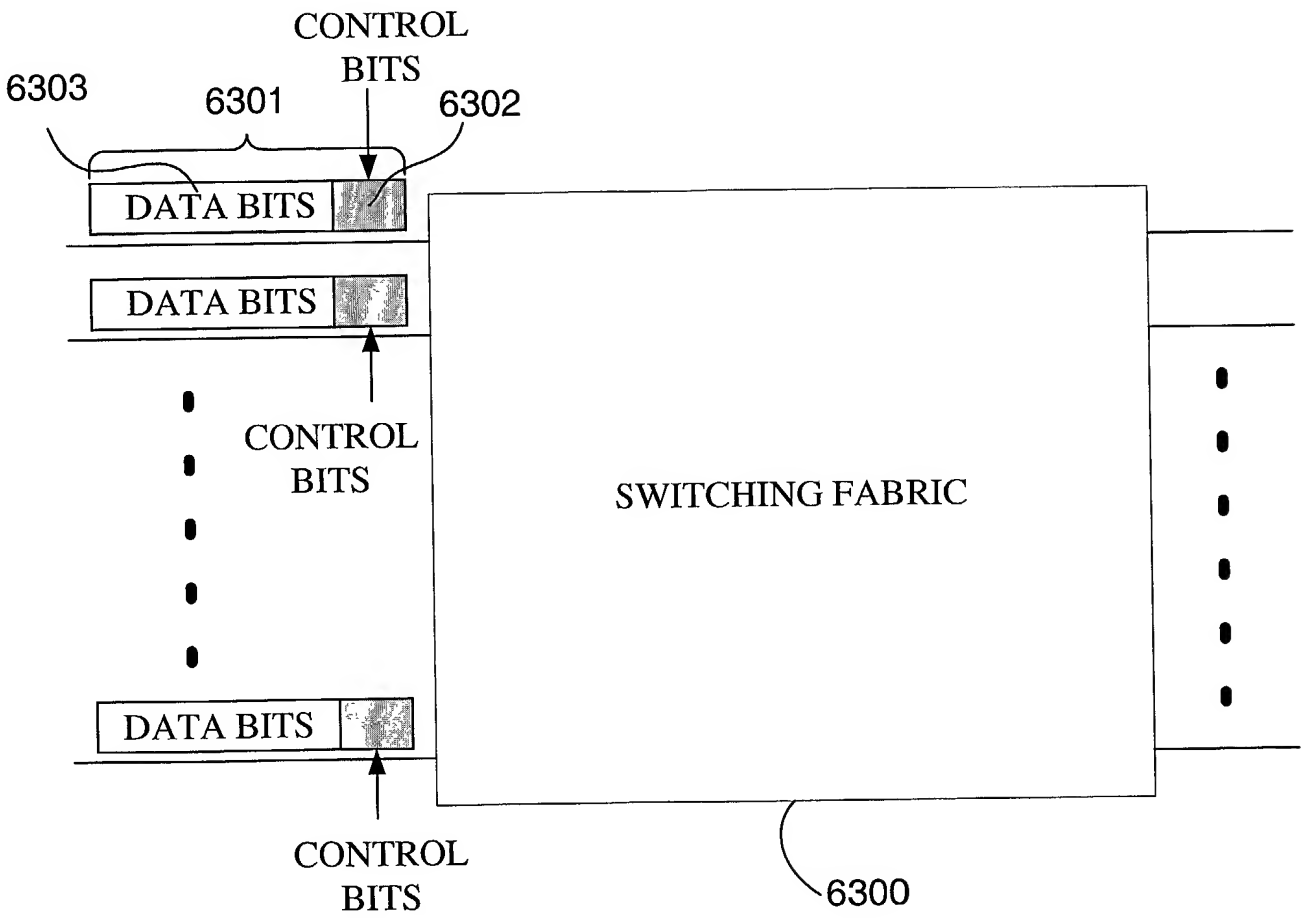

CONTROL
BITS
6303
6301
6302
DATA BITS
DATA BITS
CONTROL
BITS
SWITCHING FABRIC
DATA BITS
CONTROL
BITS
6300

FIG. 63A

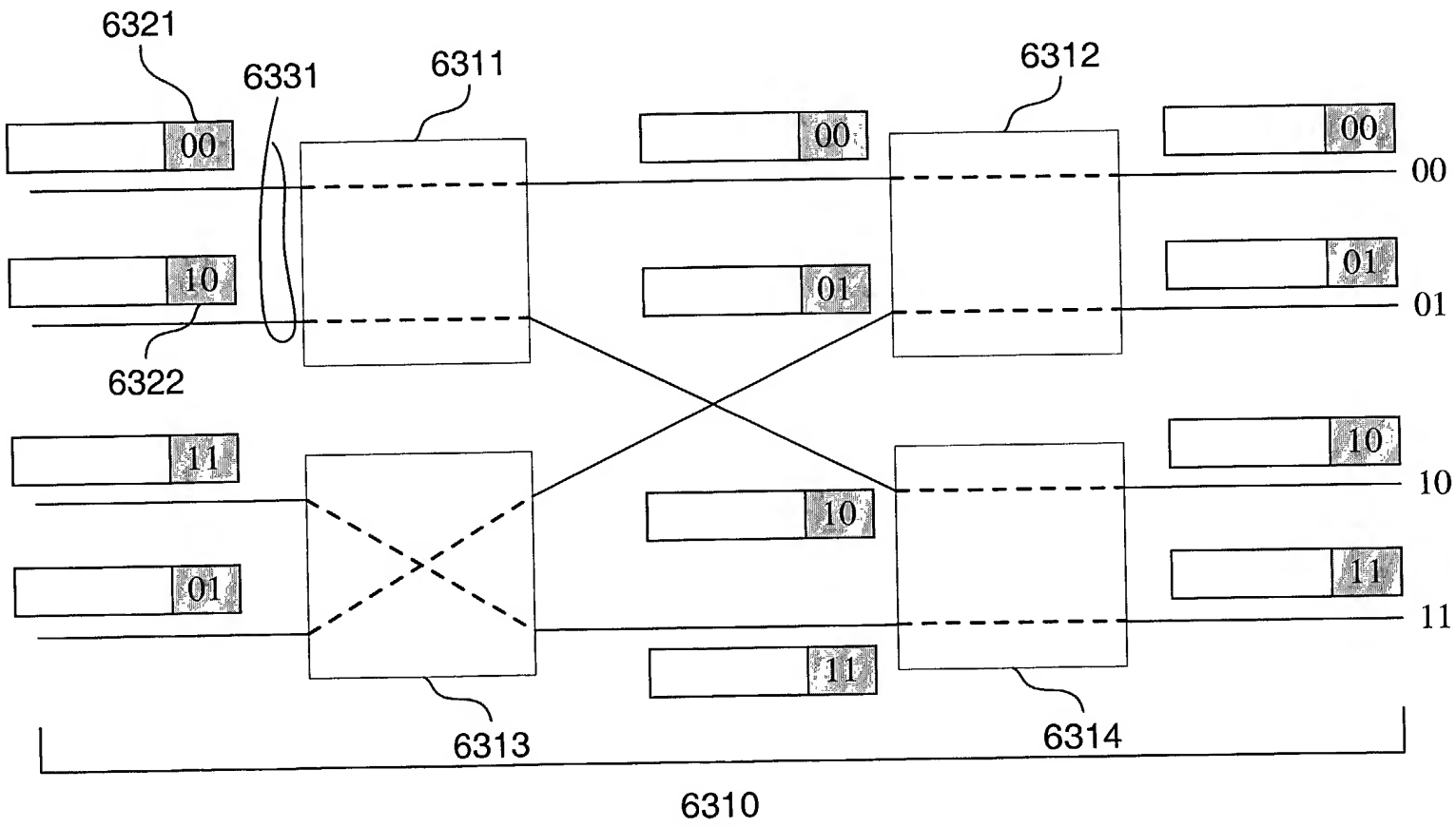


FIG. 63B

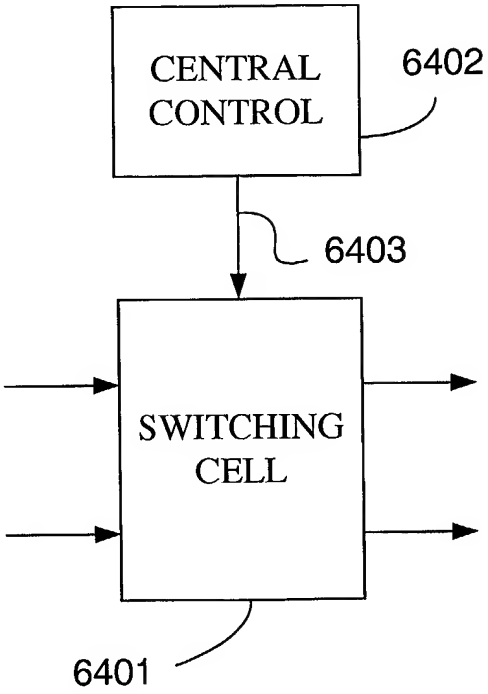


FIG. 64A

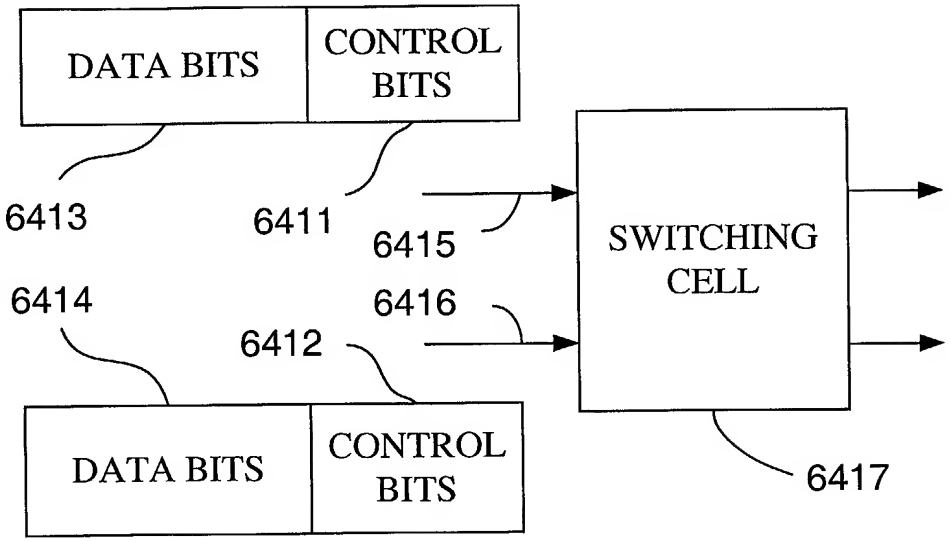


FIG. 64B

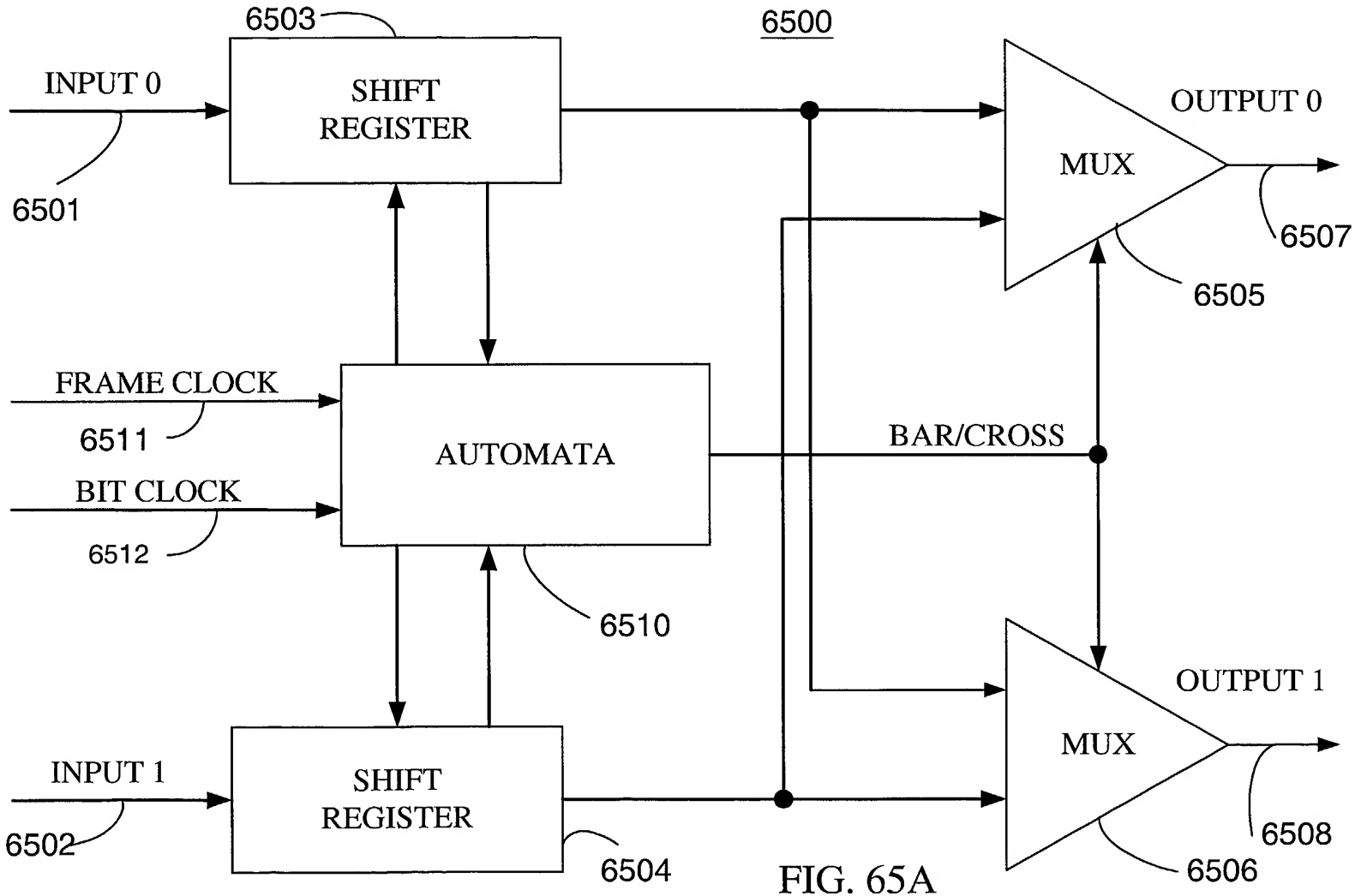

6503
6500
INPUT 0
SHIFT REGISTER
OUTPUT 0
MUX
6501
6507
6505
FRAME CLOCK
6511
AUTOMATA
BAR/CROSS
BIT CLOCK
6512
6510
OUTPUT 1
MUX
INPUT 1
SHIFT REGISTER
6502
6504
6508
6506

FIG. 65A

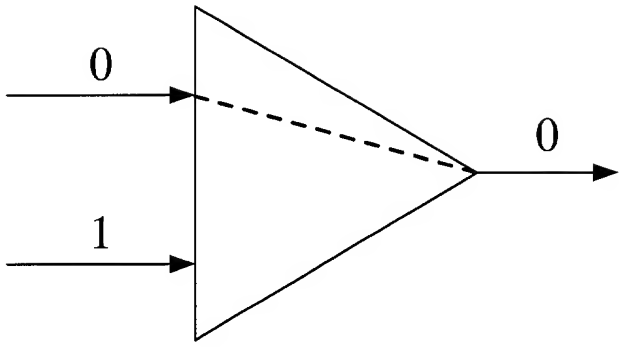


FIG. 65B

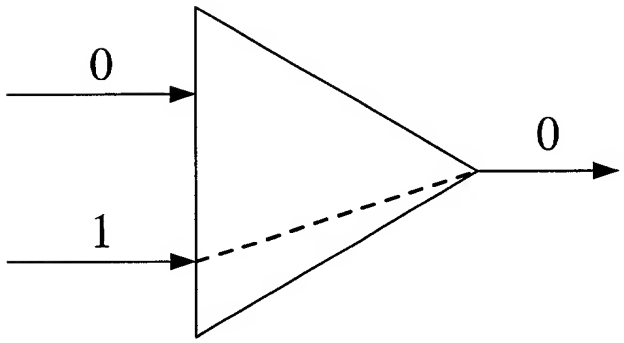


FIG. 65C

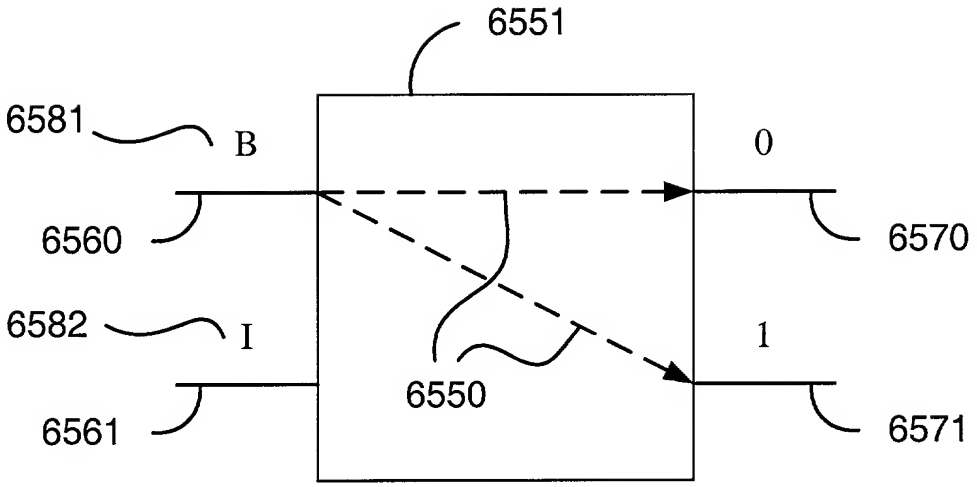


FIG. 65D

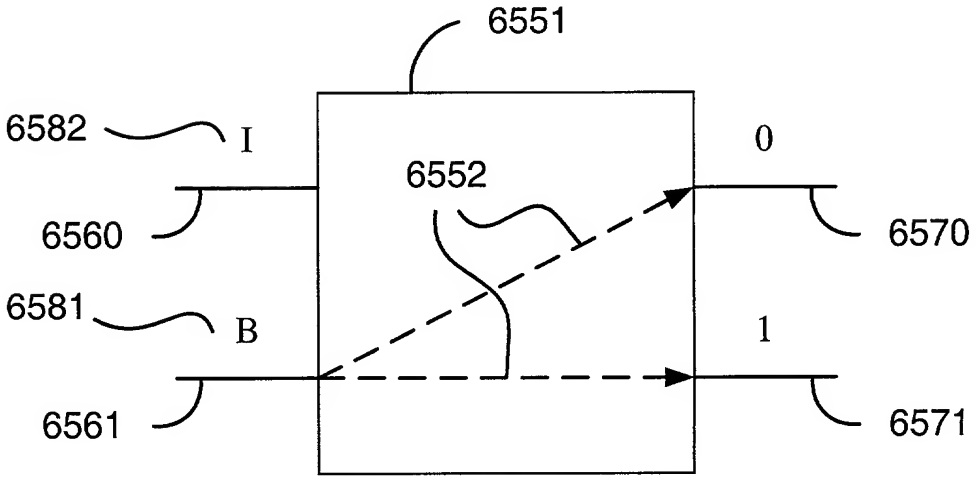


FIG. 65E

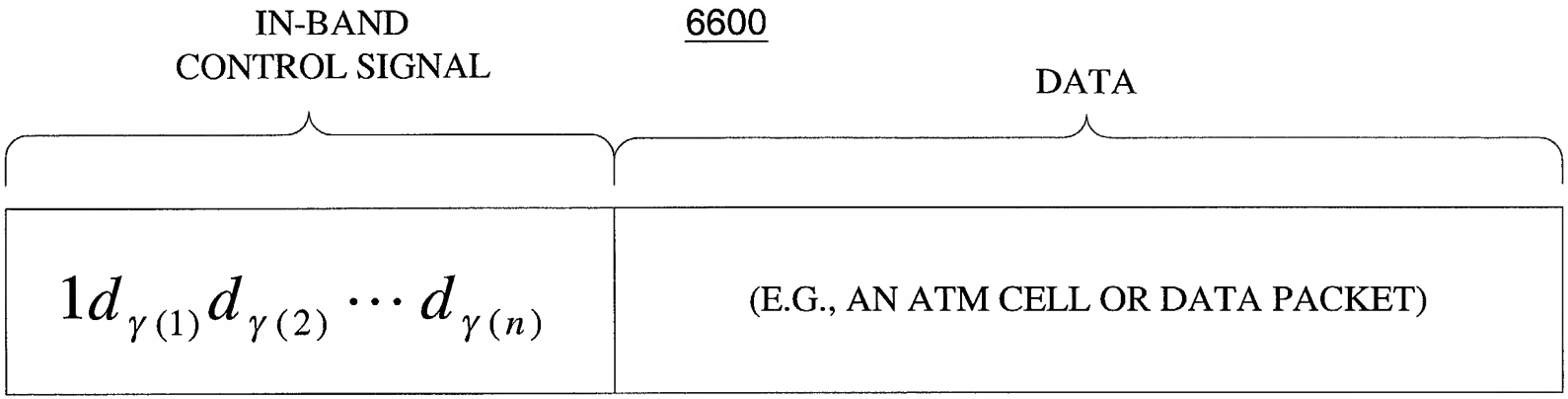

IN-BAND
CONTROL SIGNAL
6600
DATA
$1d_{\gamma(1)}d_{\gamma(2)}\cdots d_{\gamma(n)}$
(E.G., AN ATM CELL OR DATA PACKET)

FIG. 66A

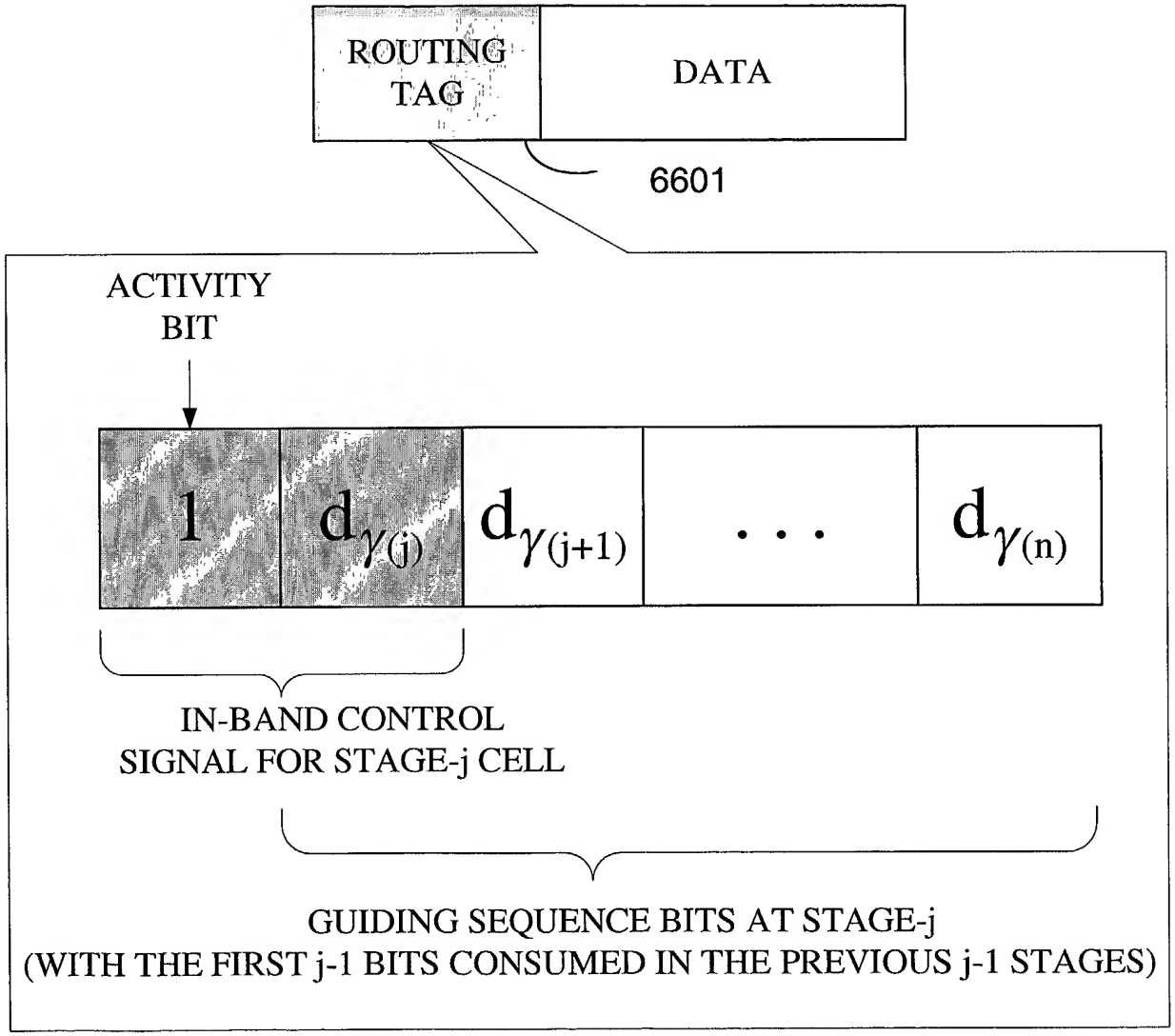

ROUTING TAG
DATA
6601
ACTIVITY BIT
1
$d_{\gamma(j)}$
$d_{\gamma(j+1)}$
. . .
$d_{\gamma(n)}$
IN-BAND CONTROL SIGNAL FOR STAGE-j CELL
GUIDING SEQUENCE BITS AT STAGE-j
(WITH THE FIRST j-1 BITS CONSUMED IN THE PREVIOUS j-1 STAGES)

FIG. 66B

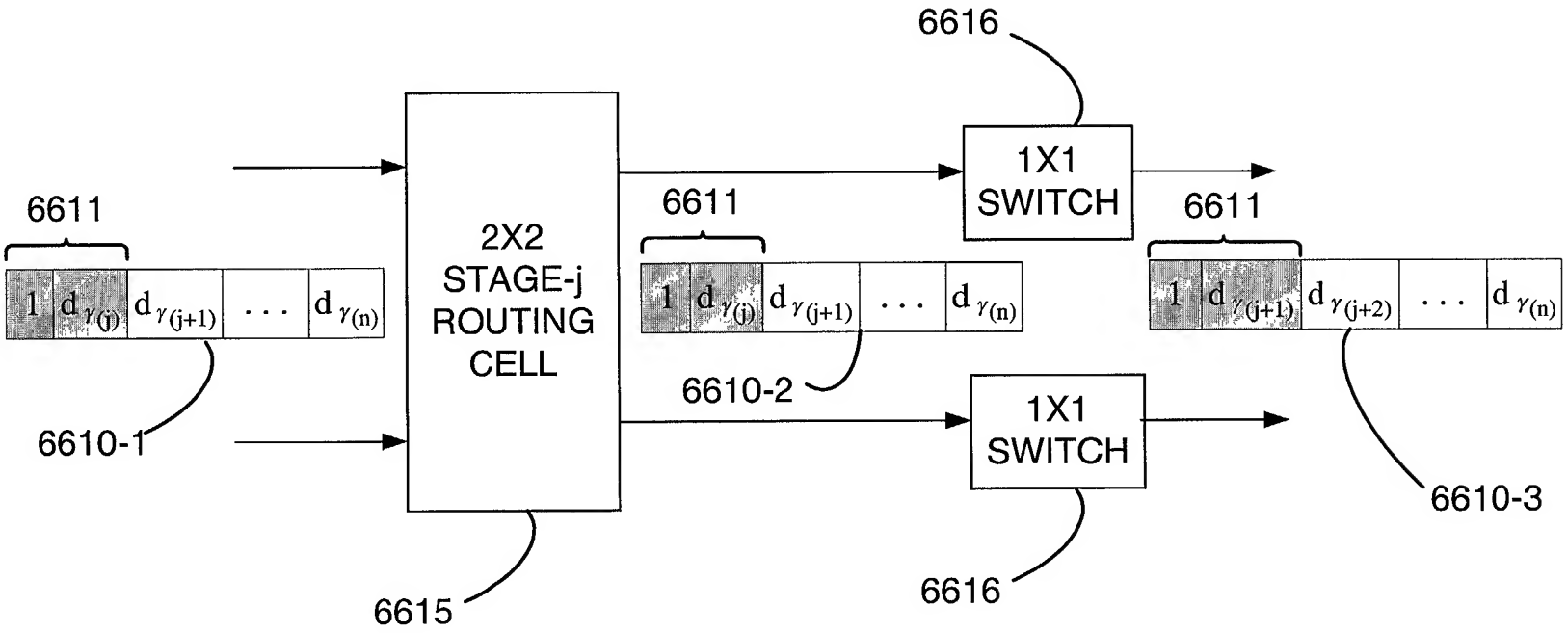

6616
6611
6611
6611
2X2
STAGE-j
ROUTING
CELL
1X1
SWITCH
1X1
SWITCH
1
d γ(j)
d γ(j+1)
. . .
d γ(n)
1
d γ(j)
d γ(j+1)
. . .
d γ(n)
1
d γ(j+1)
d γ(j+2)
. . .
d γ(n)
6610-1
6610-2
6610-3
6615
6616

FIG. 66C

FIG. 66D

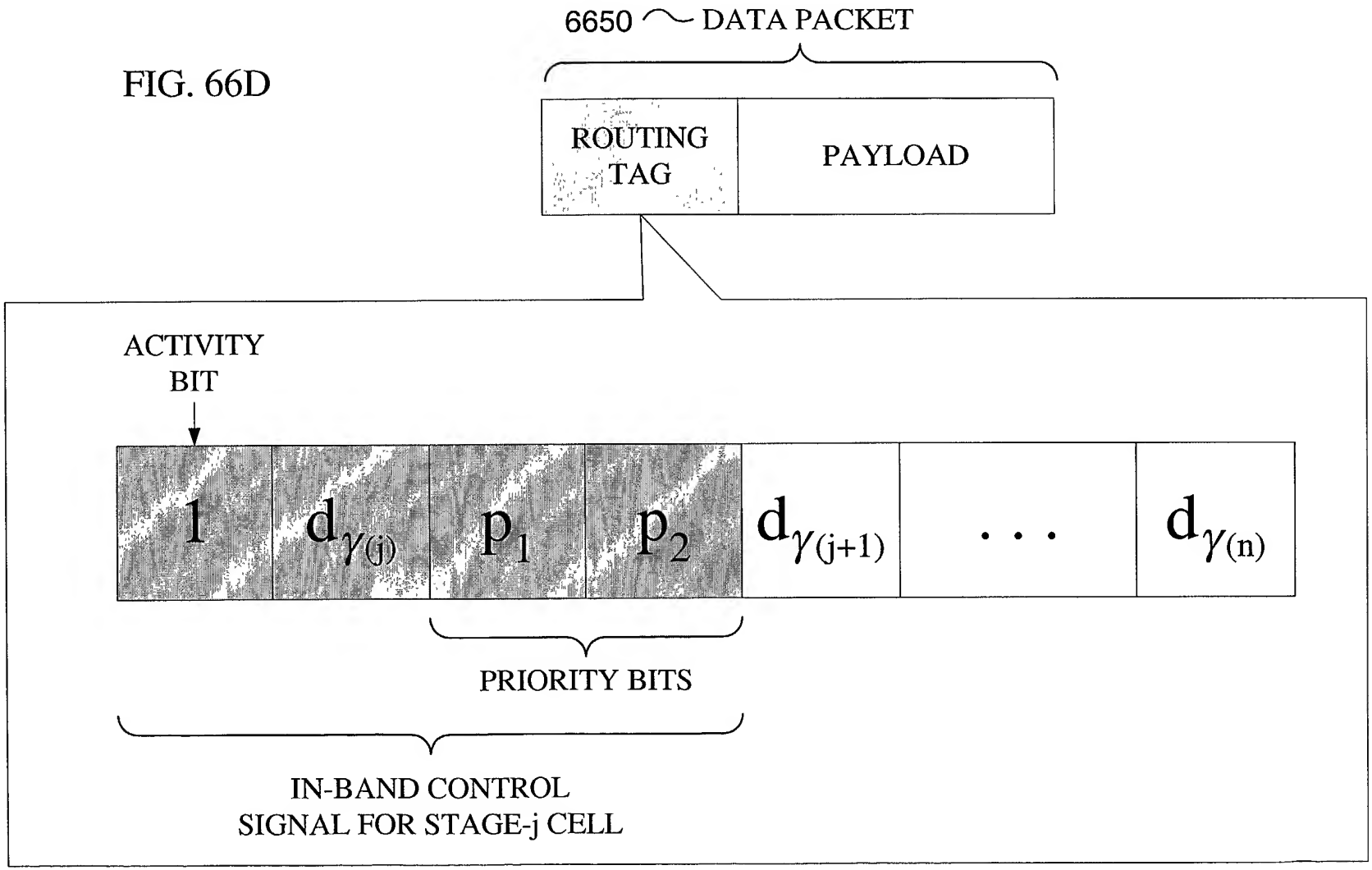

6650
DATA PACKET
ROUTING TAG
PAYLOAD
ACTIVITY BIT
1
$d_{\gamma(j)}$
p_1
p_2
$d_{\gamma(j+1)}$
. . .
$d_{\gamma(n)}$
PRIORITY BITS
IN-BAND CONTROL SIGNAL FOR STAGE-j CELL

FIG. 67A

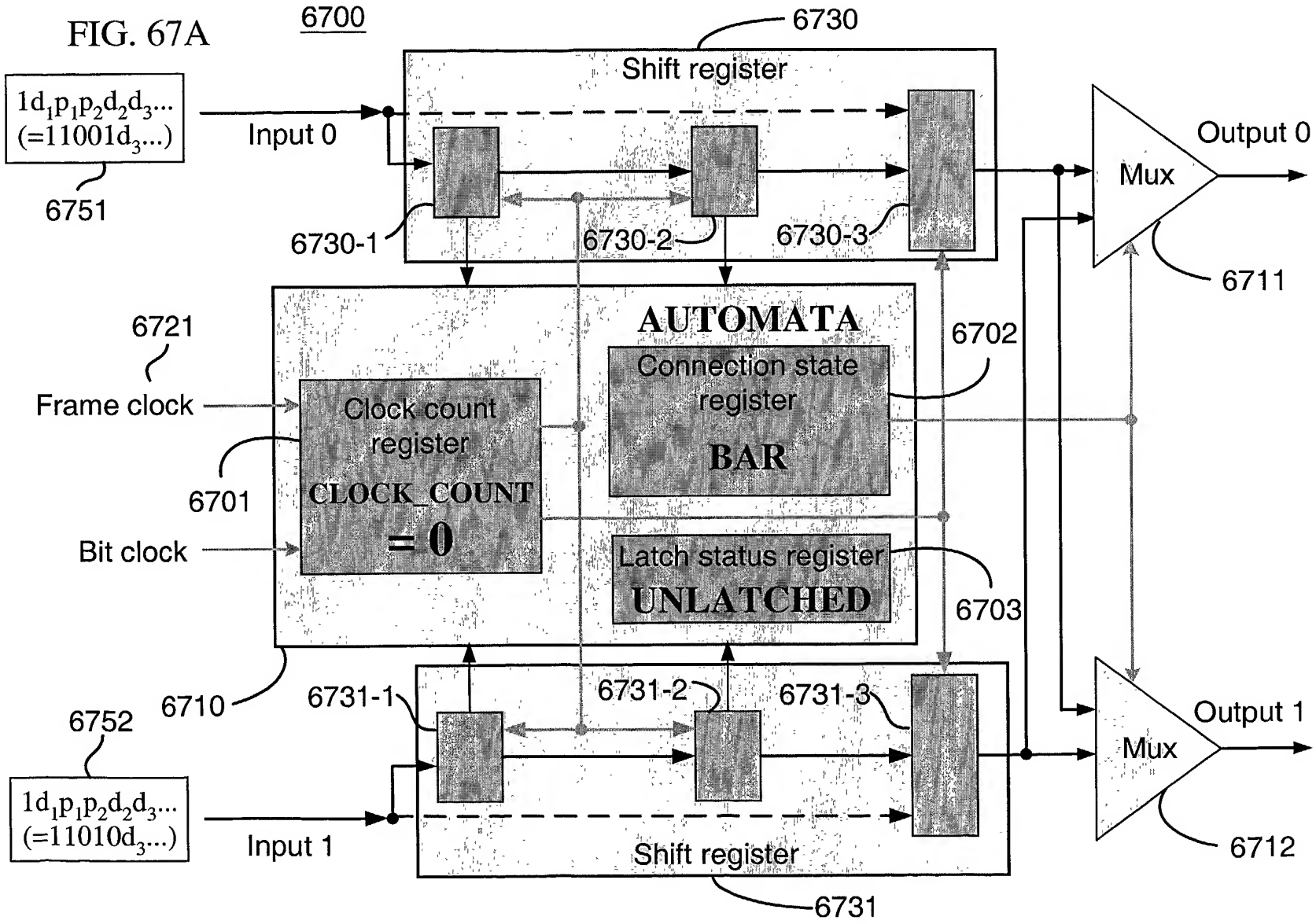

6700
6730
Shift register
$1d_1p_1p_2d_2d_3...$
$(=11001d_3...)$
Input 0
6751
6730-1
6730-2
6730-3
Output 0
Mux
6711
6721
Frame clock
AUTOMATA
6702
Connection state register
BAR
Clock count register
CLOCK_COUNT
= 0
6701
Bit clock
Latch status register
UNLATCHED
6703
6710
6731-1
6731-2
6731-3
6752
Output 1
Mux
$1d_1p_1p_2d_2d_3...$
$(=11010d_3...)$
Input 1
6712
Shift register
6731

FIG. 67B

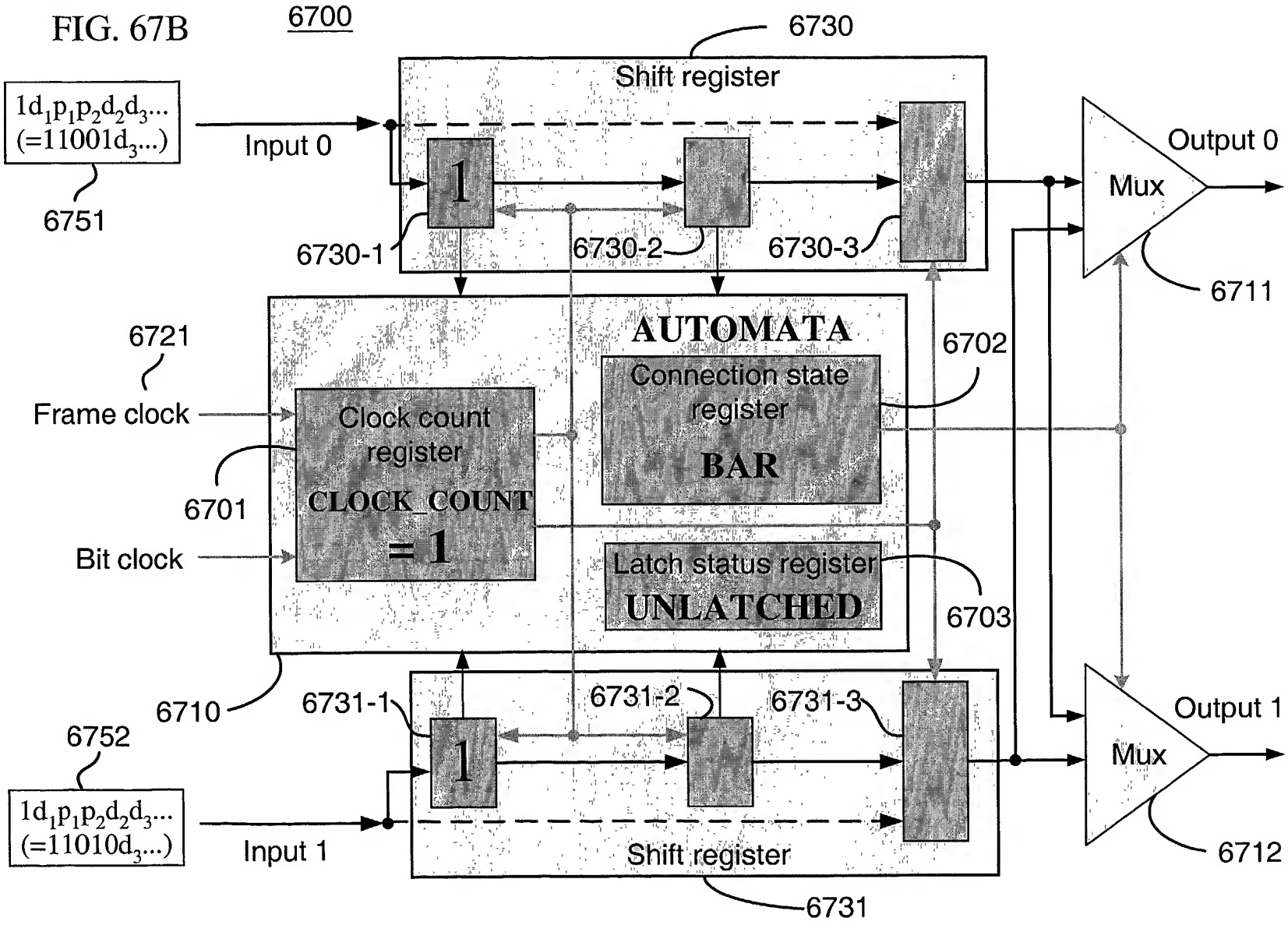

6700
6730
Shift register
$1d_1p_1p_2d_2d_3...$
$(=11001d_3...)$
Input 0
6751
1
6730-1
6730-2
6730-3
Output 0
Mux
6711
6721
Frame clock
AUTOMATA
6702
Connection state register
BAR
Clock count register
CLOCK_COUNT
= 1
6701
Bit clock
Latch status register
UNLATCHED
6703
6710
6731-1
6731-2
6731-3
Output 1
Mux
6752
$1d_1p_1p_2d_2d_3...$
$(=11010d_3...)$
Input 1
1
Shift register
6731
6712

FIG. 67C

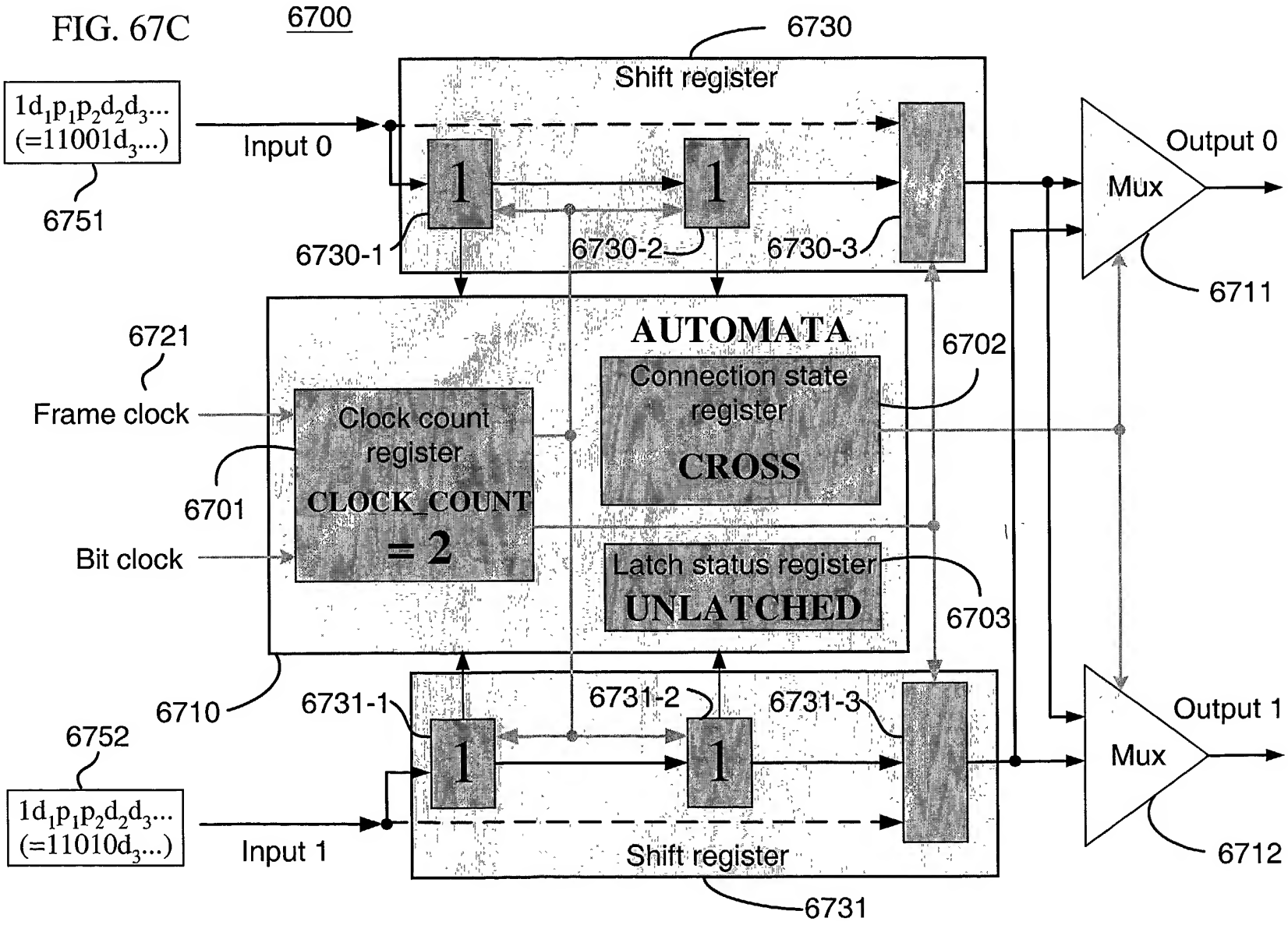

6700
6730
Shift register
$1d_1p_1p_2d_2d_3...$
$(=11001d_3...)$
Input 0
6751
1
1
6730-1
6730-2
6730-3
Output 0
Mux
6711
6721
Frame clock
AUTOMATA
6702
Connection state register
CROSS
Clock count register
CLOCK_COUNT
= 2
6701
Bit clock
Latch status register
UNLATCHED
6703
6710
6731-1
6731-2
6731-3
Output 1
Mux
6752
$1d_1p_1p_2d_2d_3...$
$(=11010d_3...)$
Input 1
Shift register
6731
6712

FIG. 67D

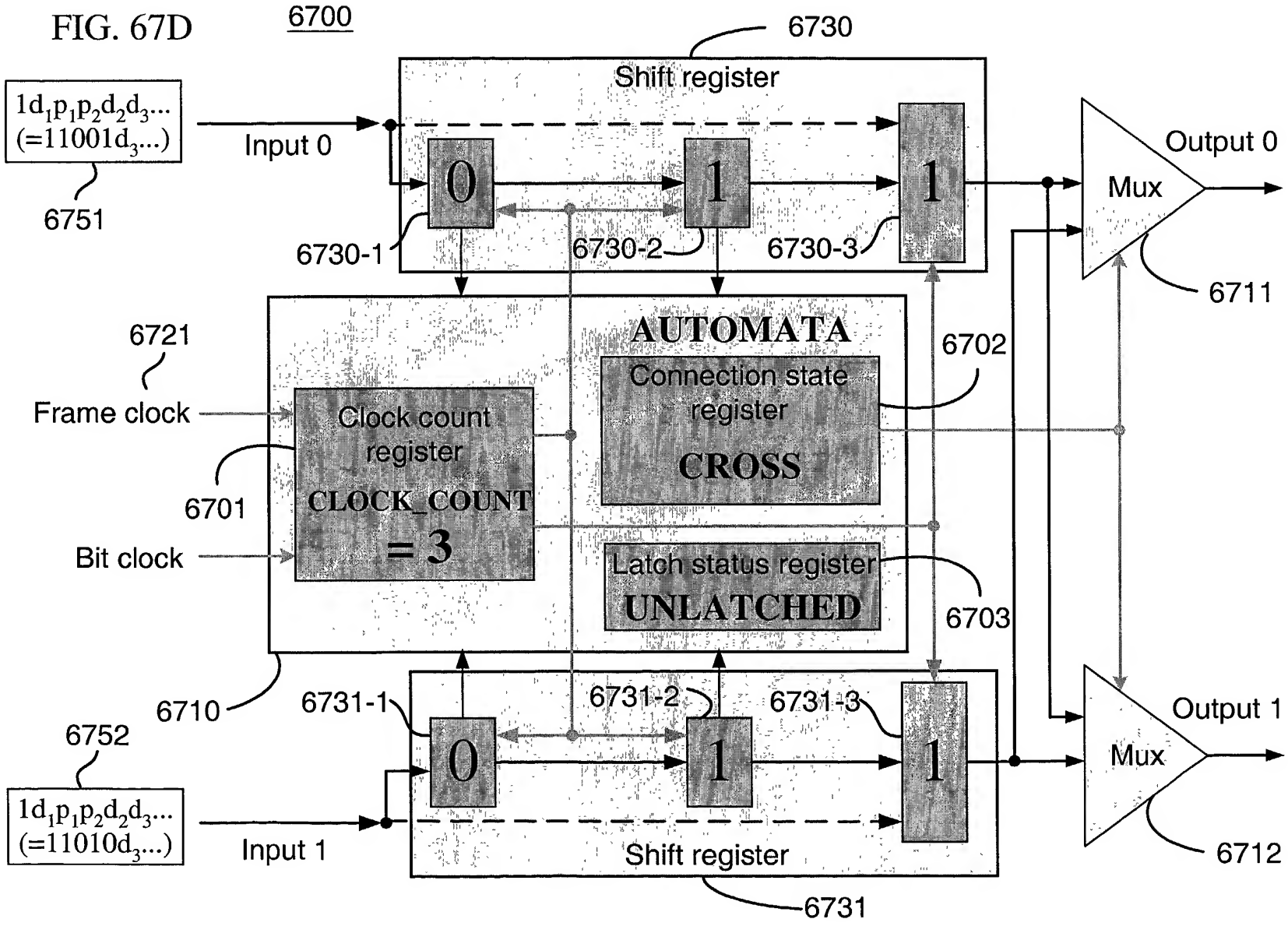

6700
6730
Shift register
$1d_1p_1p_2d_2d_3...$
$(=11001d_3...)$
Input 0
6751
0
1
1
6730-1
6730-2
6730-3
Output 0
Mux
6711
6721
Frame clock
AUTOMATA
6702
Connection state register
CROSS
Clock count register
CLOCK_COUNT
= 3
6701
Bit clock
Latch status register
UNLATCHED
6703
6710
6731-1
6731-2
6731-3
Output 1
6752
$1d_1p_1p_2d_2d_3...$
$(=11010d_3...)$
Input 1
Shift register
6731
Mux
6712

FIG. 67E

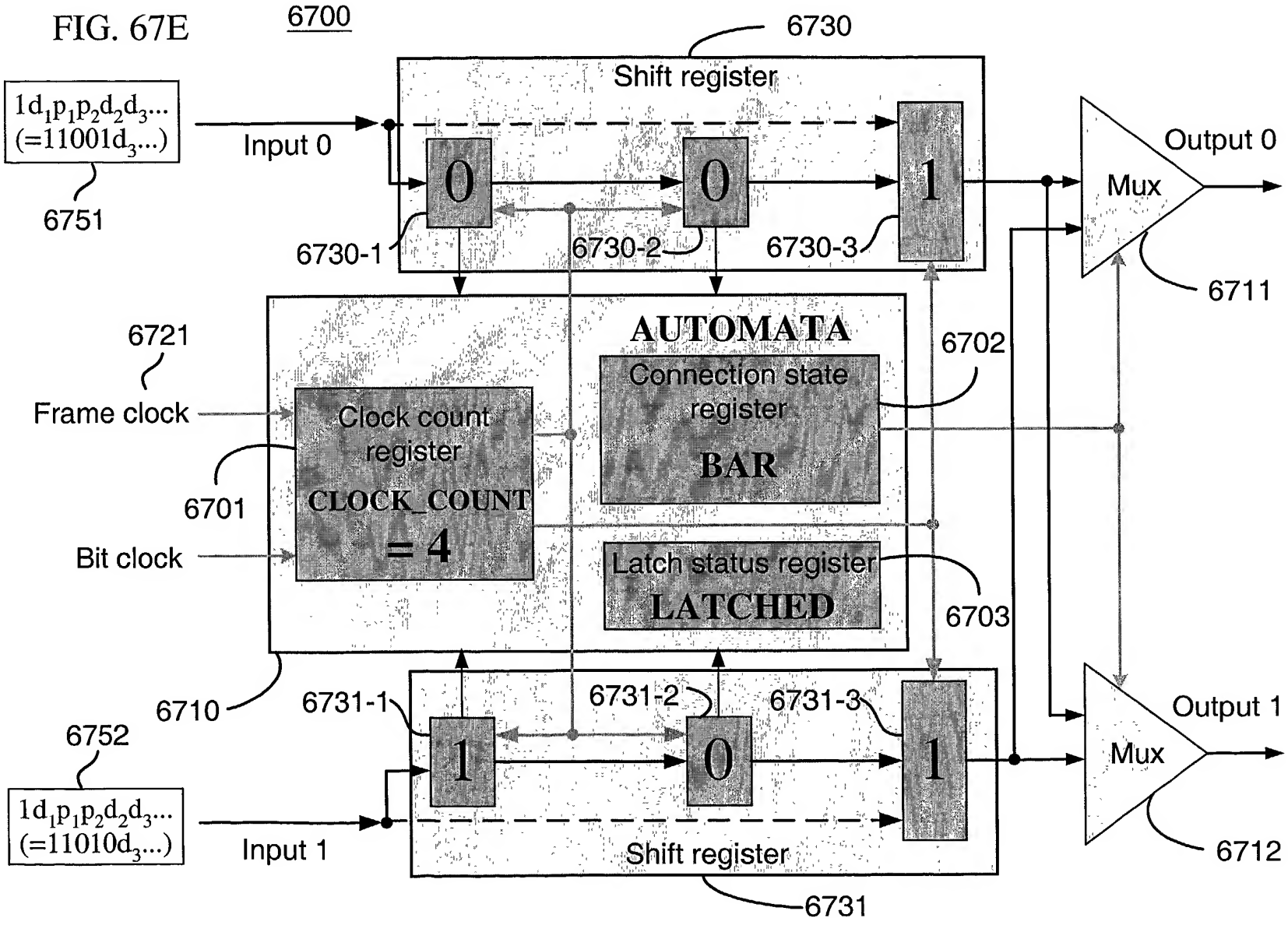
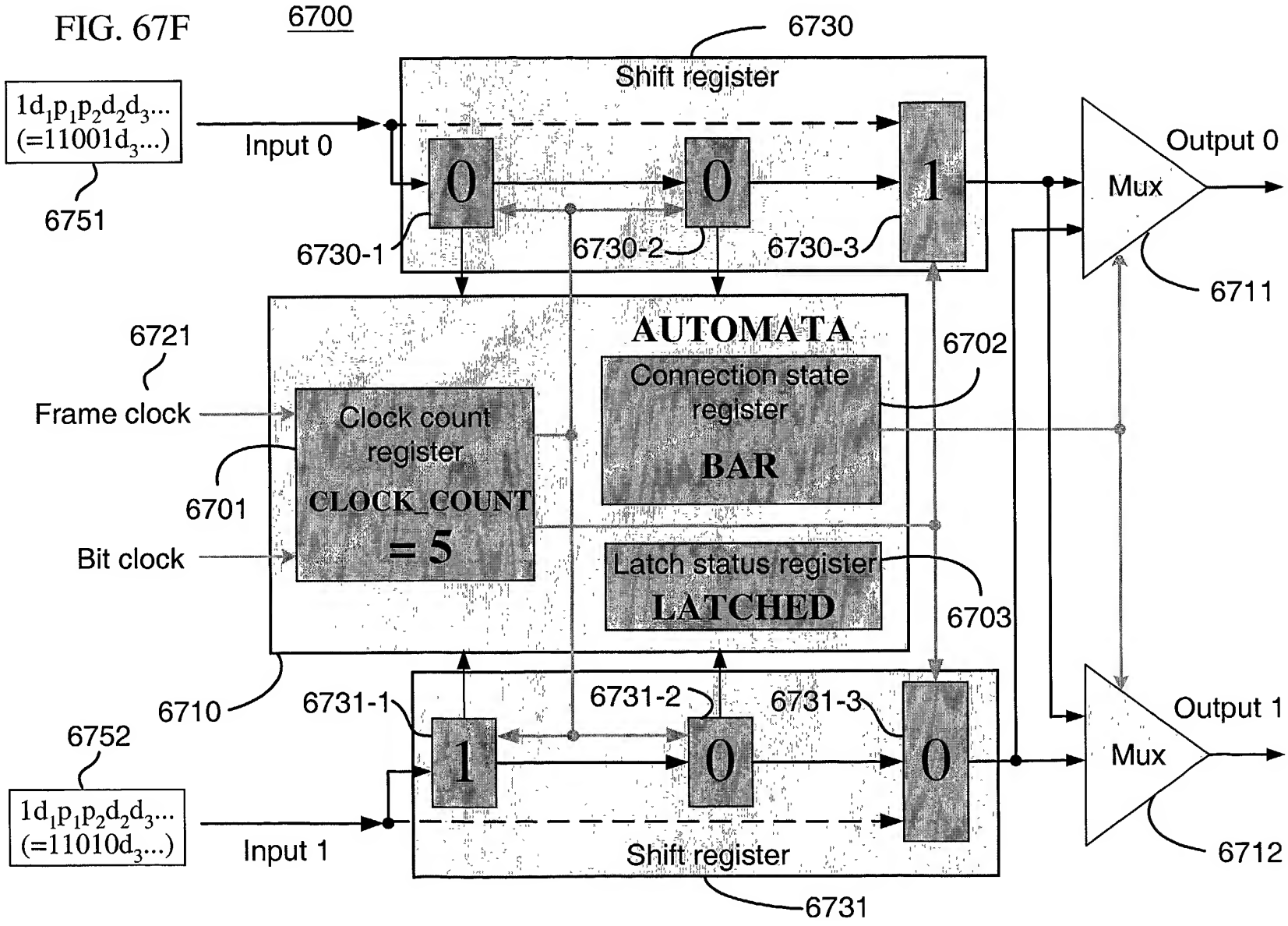

6700
6730
Shift register
$1d_1p_1p_2d_2d_3...$
$(=11001d_3...)$
Input 0
6751
0
0
1
6730-1
6730-2
6730-3
Output 0
Mux
6711
6721
Frame clock
AUTOMATA
6702
Connection state register
BAR
Clock count register
CLOCK_COUNT
= 4
6701
Bit clock
Latch status register
LATCHED
6703
6710
6731-1
6731-2
6731-3
Output 1
Mux
6752
$1d_1p_1p_2d_2d_3...$
$(=11010d_3...)$
Input 1
1
0
1
Shift register
6731
6712

FIG. 67F


6700
6730
Shift register
$1d_1p_1p_2d_2d_3...$
$(=11001d_3...)$
Input 0
6751
0
0
1
6730-1
6730-2
6730-3
Output 0
Mux
6711
AUTOMATA
6721
Frame clock
Clock count register
CLOCK_COUNT
= 5
6701
Bit clock
Connection state register
BAR
6702
Latch status register
LATCHED
6703
6710
6731-1
6731-2
6731-3
1
0
0
Output 1
Mux
6712
6752
$1d_1p_1p_2d_2d_3...$
$(=11010d_3...)$
Input 1
Shift register
6731

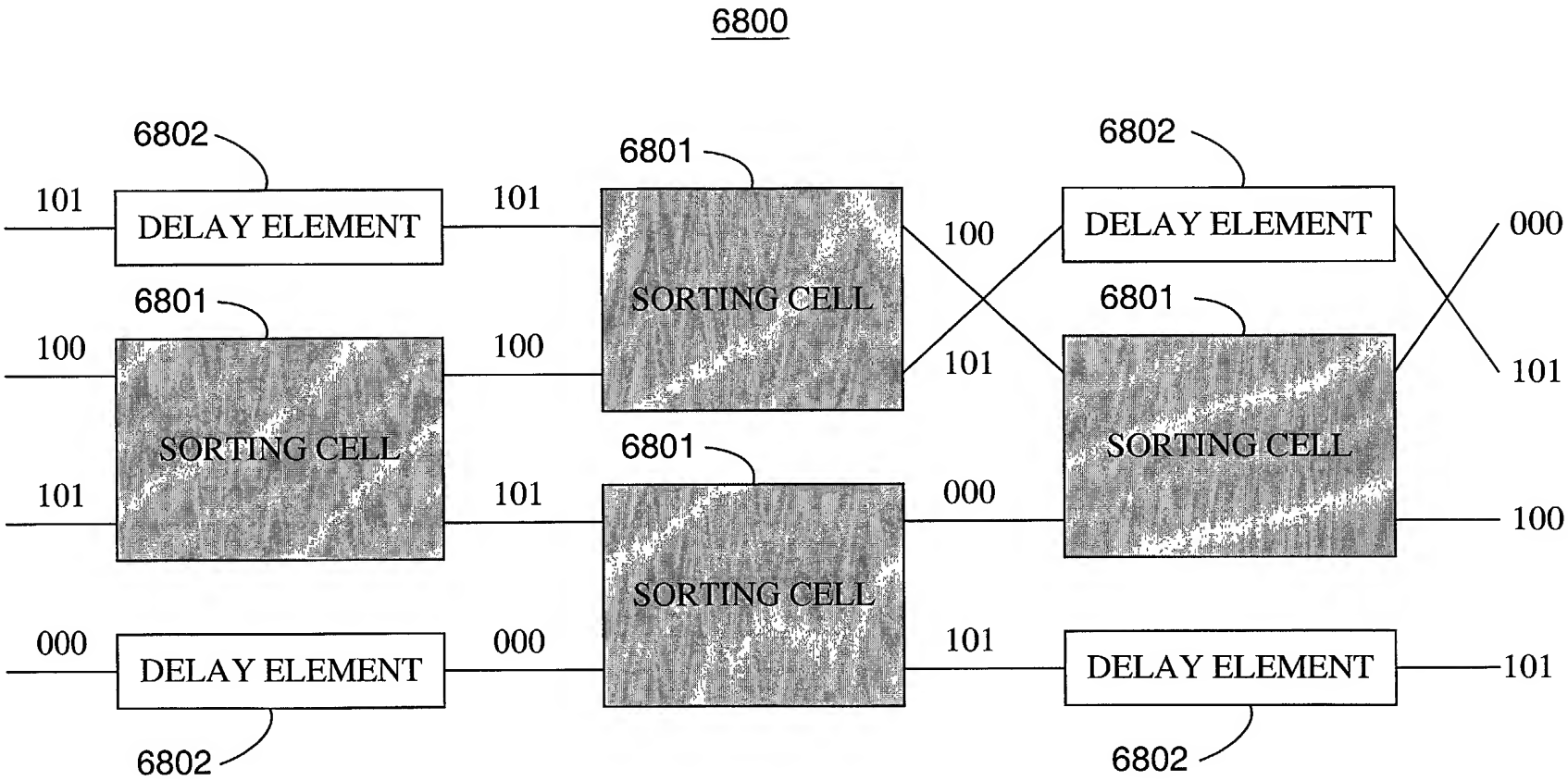
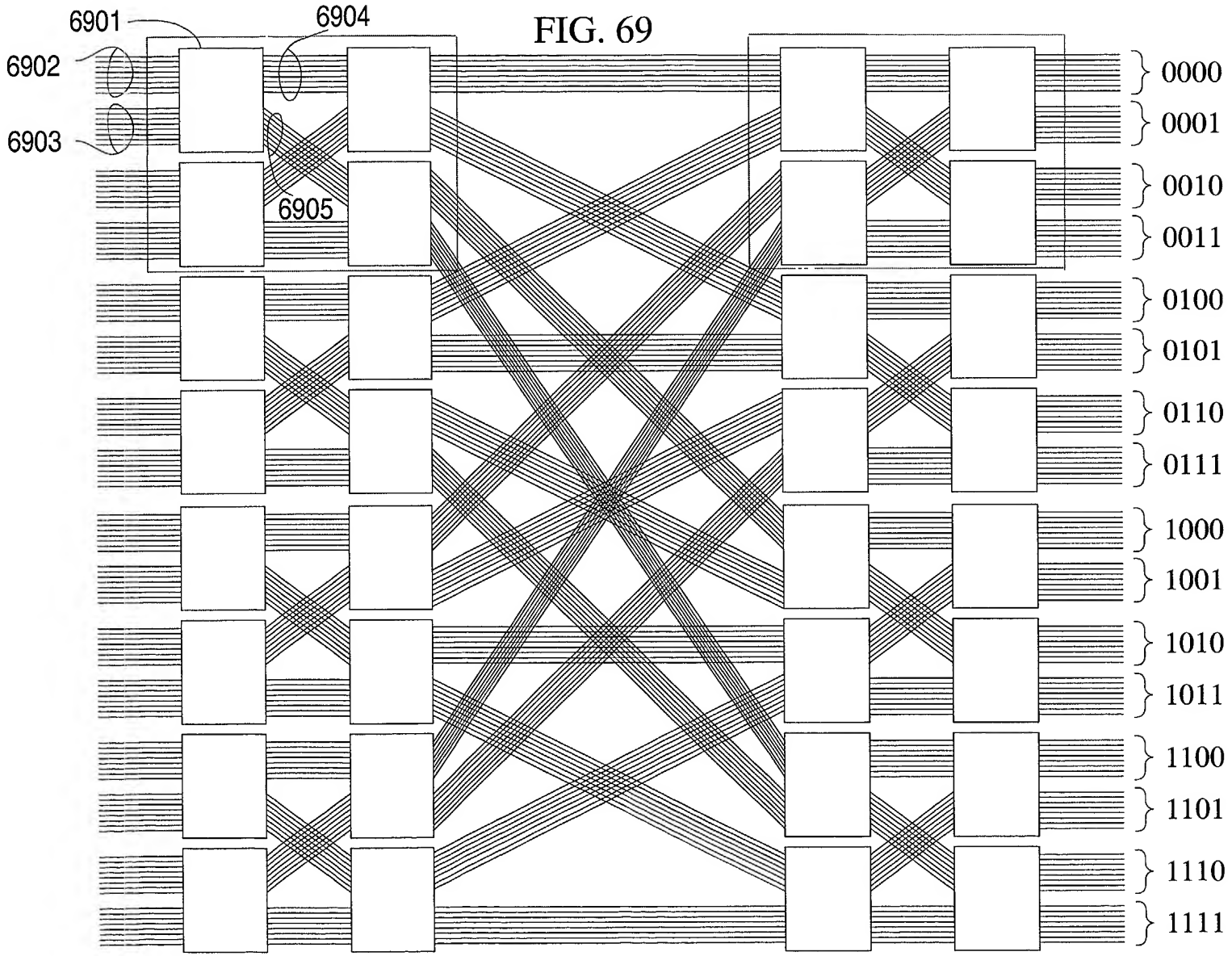

6800
6802
6801
6802
101
DELAY ELEMENT
101
SORTING CELL
100
DELAY ELEMENT
000
6801
6801
100
100
SORTING CELL
101
SORTING CELL
101
6801
101
101
000
100
SORTING CELL
000
DELAY ELEMENT
000
101
DELAY ELEMENT
101
6802
6802

FIG. 68

FIG. 69


6901
6904
6902
6903
6905
0000
0001
0010
0011
0100
0101
0110
0111
1000
1001
1010
1011
1100
1101
1110
1111

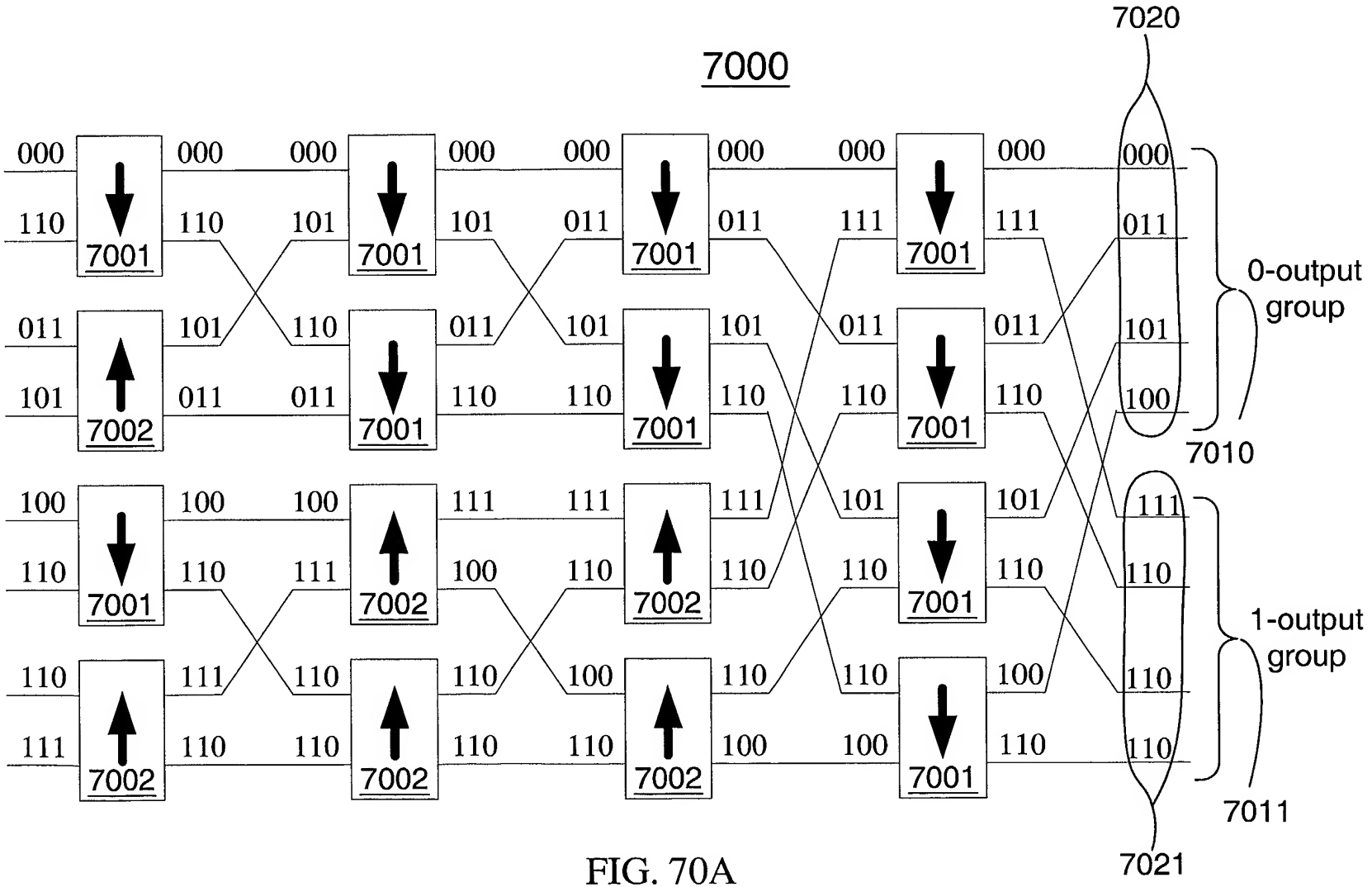

7000
7020
7001
7002
0-output group
1-output group
7010
7011
7021

FIG. 70A

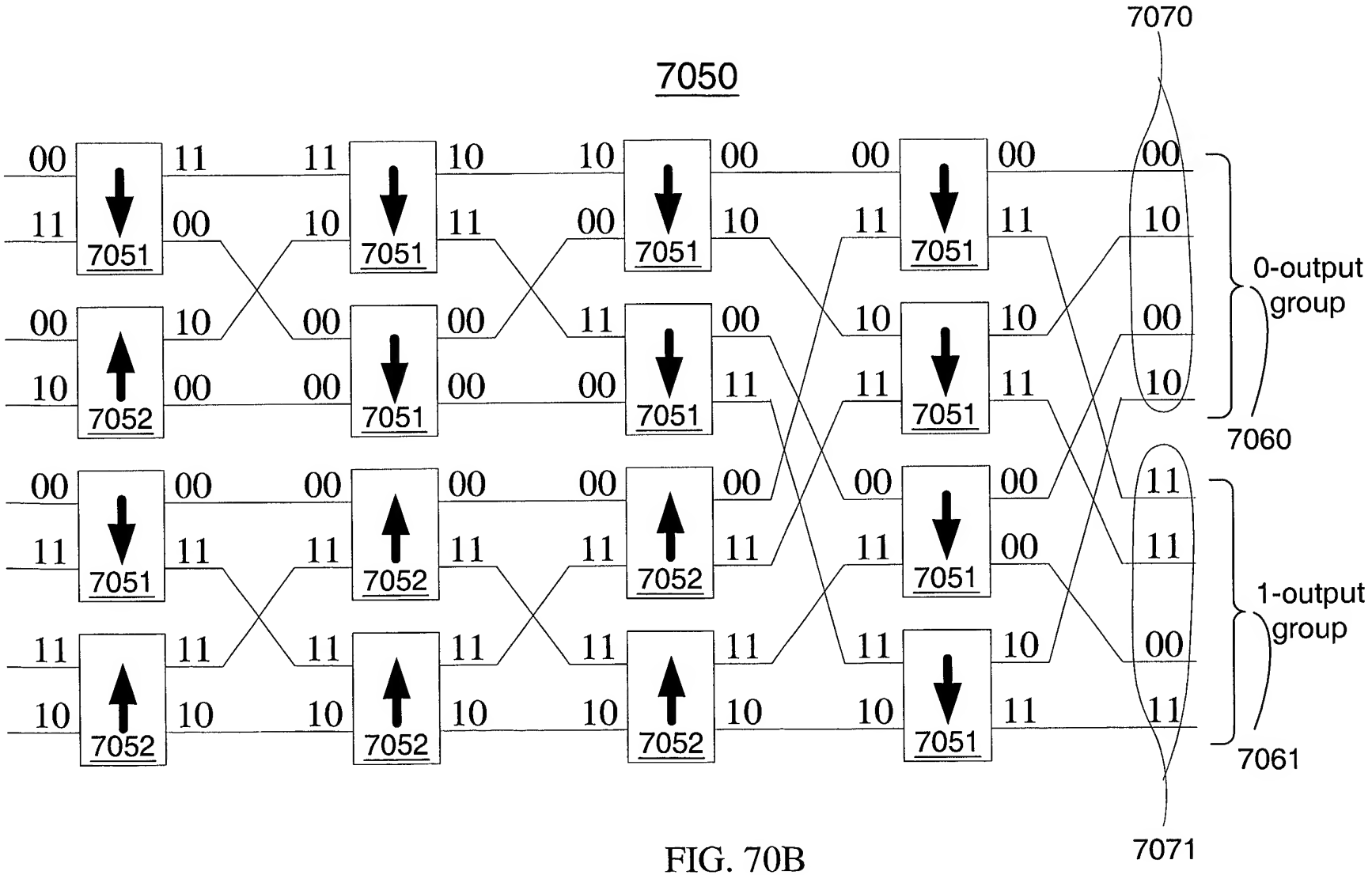

7050
7070
7051
7052
0-output group
1-output group
7060
7061
7071

FIG. 70B

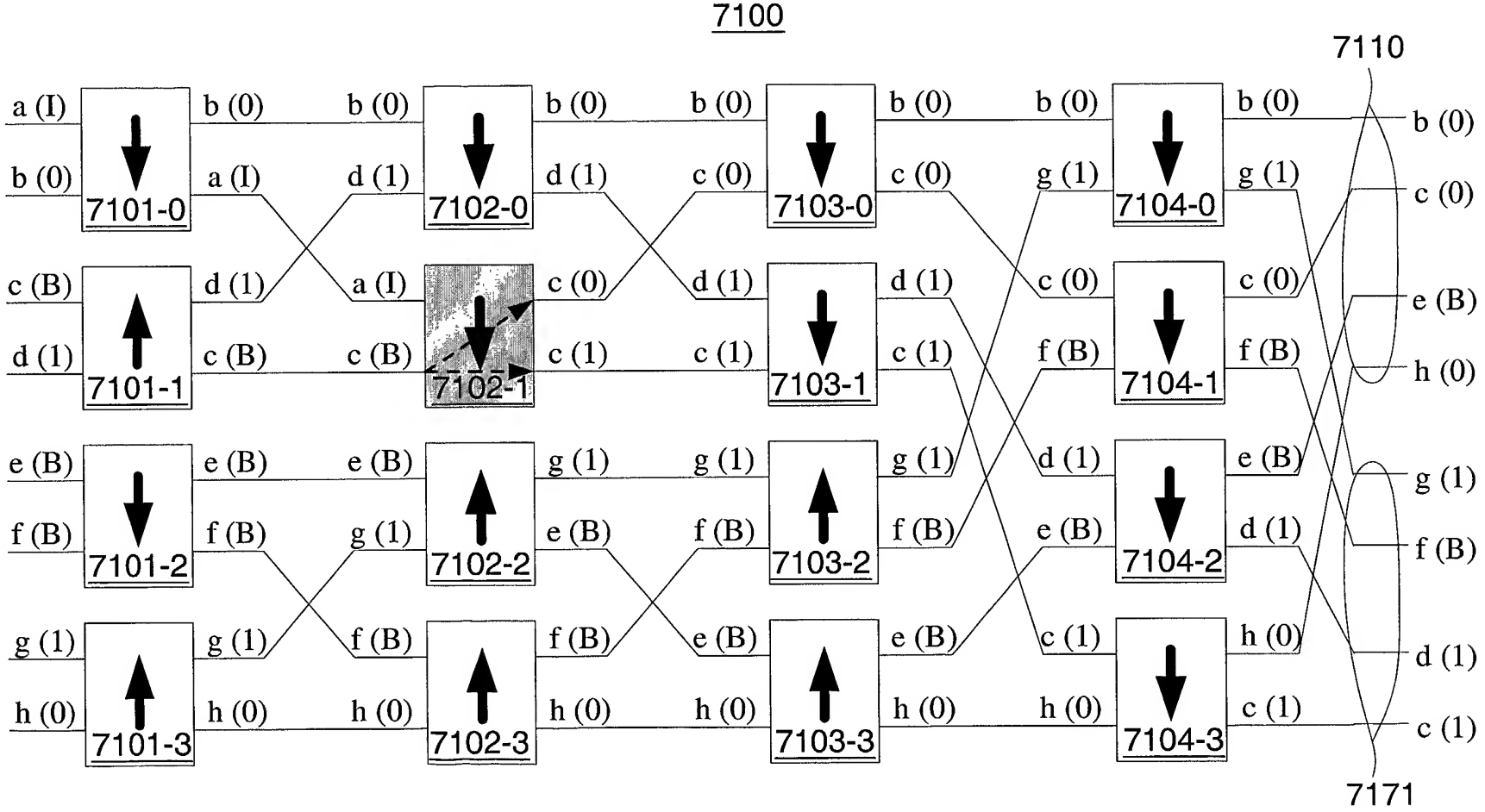

7100
7110
7171
a (I)
b (0)
c (B)
d (1)
e (B)
f (B)
g (1)
h (0)
7101-0
7101-1
7101-2
7101-3
7102-0
7102-1
7102-2
7102-3
7103-0
7103-1
7103-2
7103-3
7104-0
7104-1
7104-2
7104-3

FIG. 71A

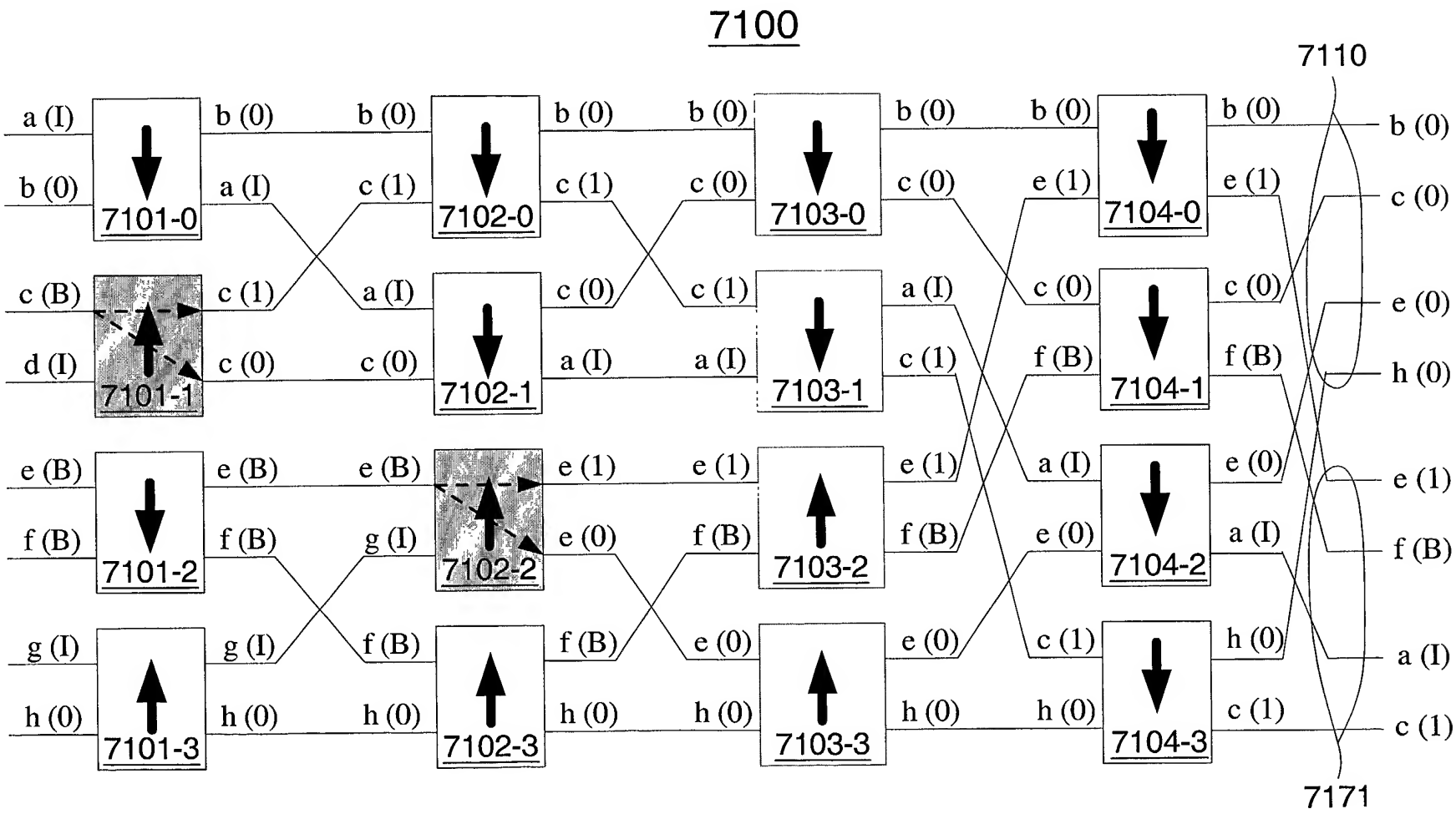

7100
7110
7171
7101-0
7101-1
7101-2
7101-3
7102-0
7102-1
7102-2
7102-3
7103-0
7103-1
7103-2
7103-3
7104-0
7104-1
7104-2
7104-3
a (I)
b (0)
c (B)
d (I)
e (B)
f (B)
g (I)
h (0)
c (1)
c (0)
e (1)
e (0)

FIG. 71B

7200

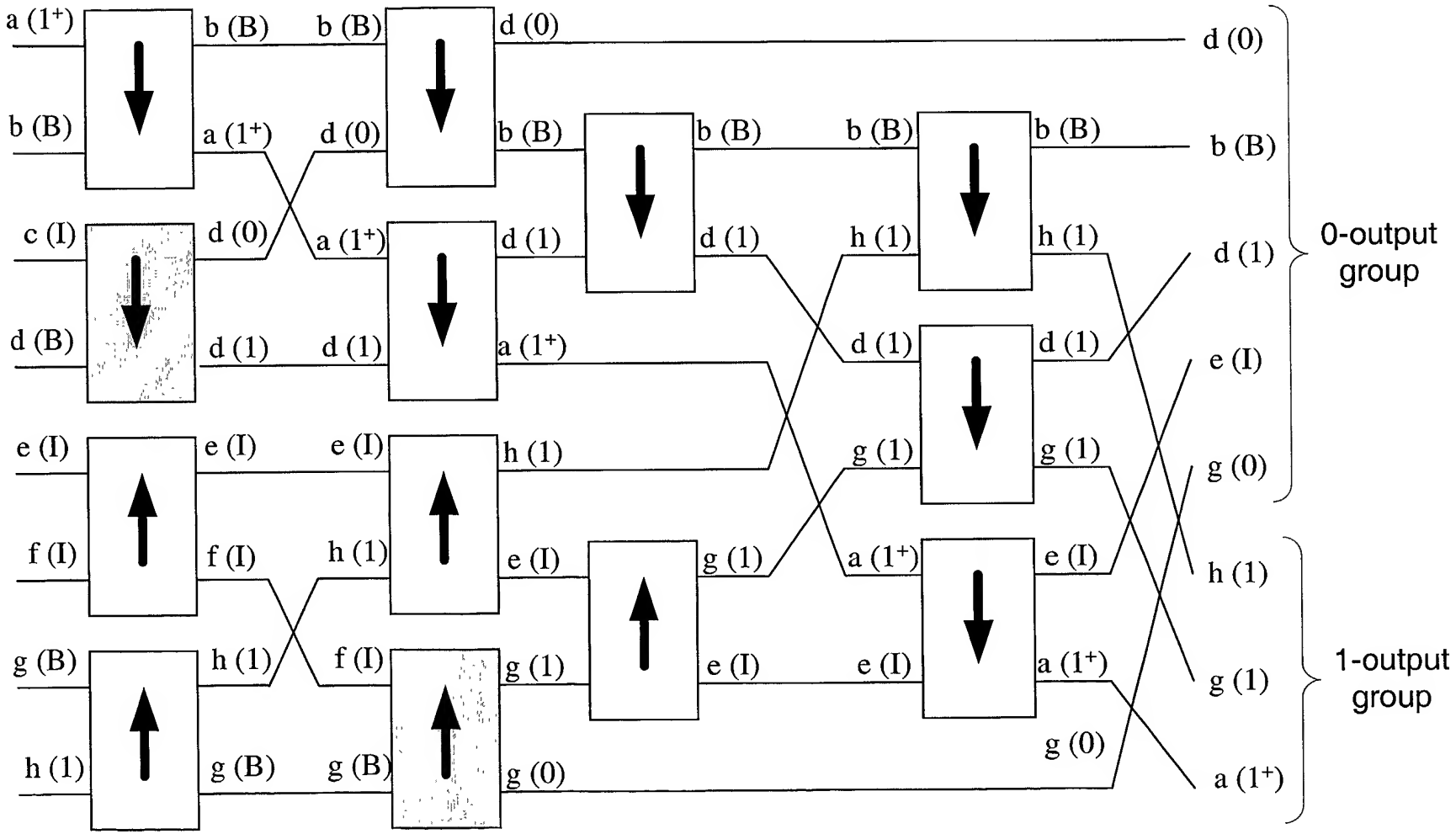

a (1+)
b (B)
c (I)
d (B)
e (I)
f (I)
g (B)
h (1)
b (B)
a (1+)
d (0)
d (1)
e (I)
f (I)
h (1)
g (B)
b (B)
d (0)
a (1+)
d (1)
e (I)
h (1)
f (I)
g (1)
g (B)
d (0)
b (B)
d (1)
a (1+)
h (1)
e (I)
g (1)
g (0)
b (B)
d (1)
h (1)
g (1)
e (I)
a (1+)
e (I)
g (1)
b (B)
h (1)
d (1)
g (1)
a (1+)
e (I)
a (1+)
g (0)
d (0)
b (B)
d (1)
e (I)
g (0)
h (1)
g (1)
a (1+)
0-output group
1-output group

FIG. 72A

7200

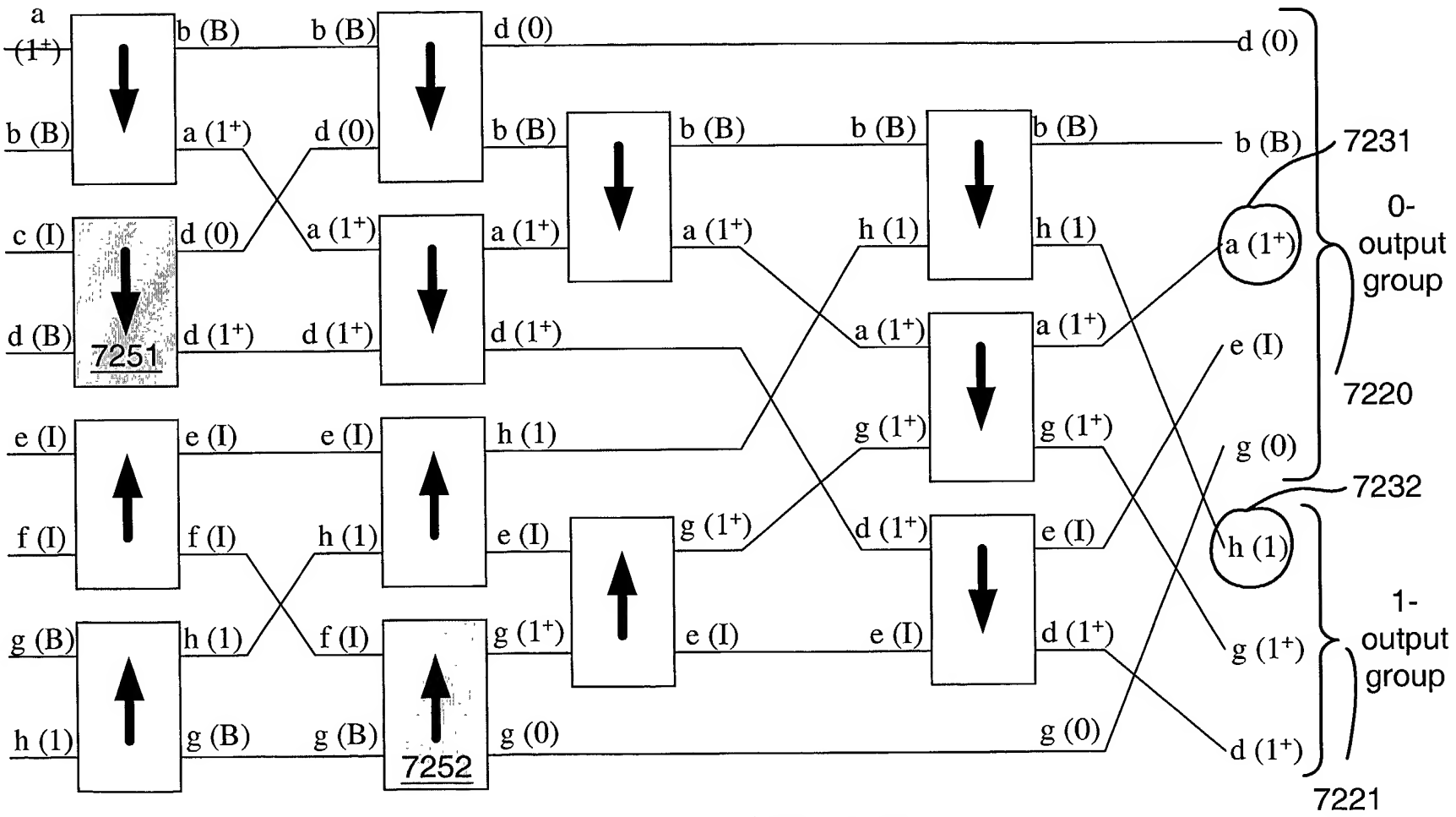

a (1+)
b (B)
c (I)
d (B)
e (I)
f (I)
g (B)
h (1)
7251
7252
7231
0-output group
7220
7232
1-output group
7221

FIG. 72B

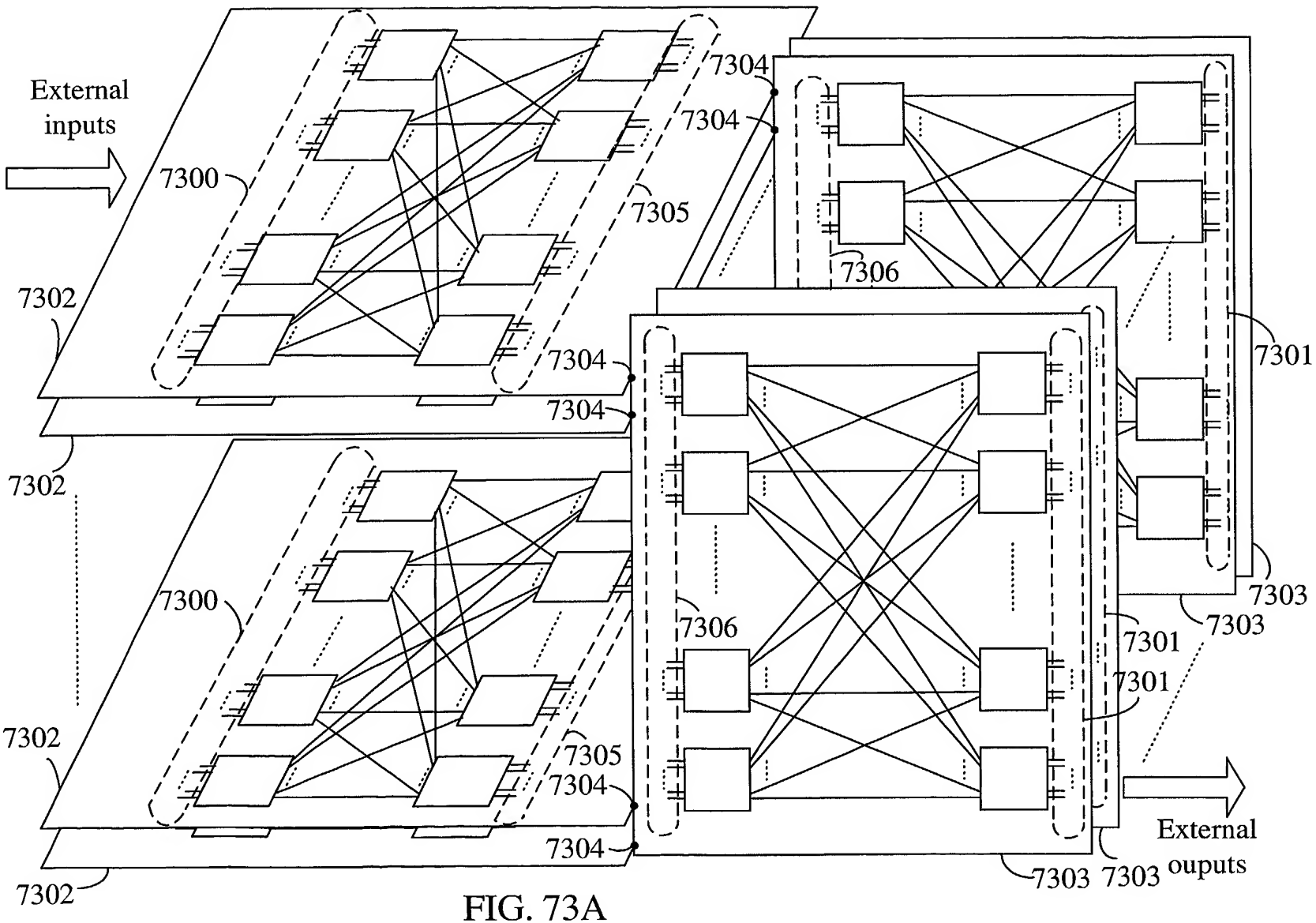
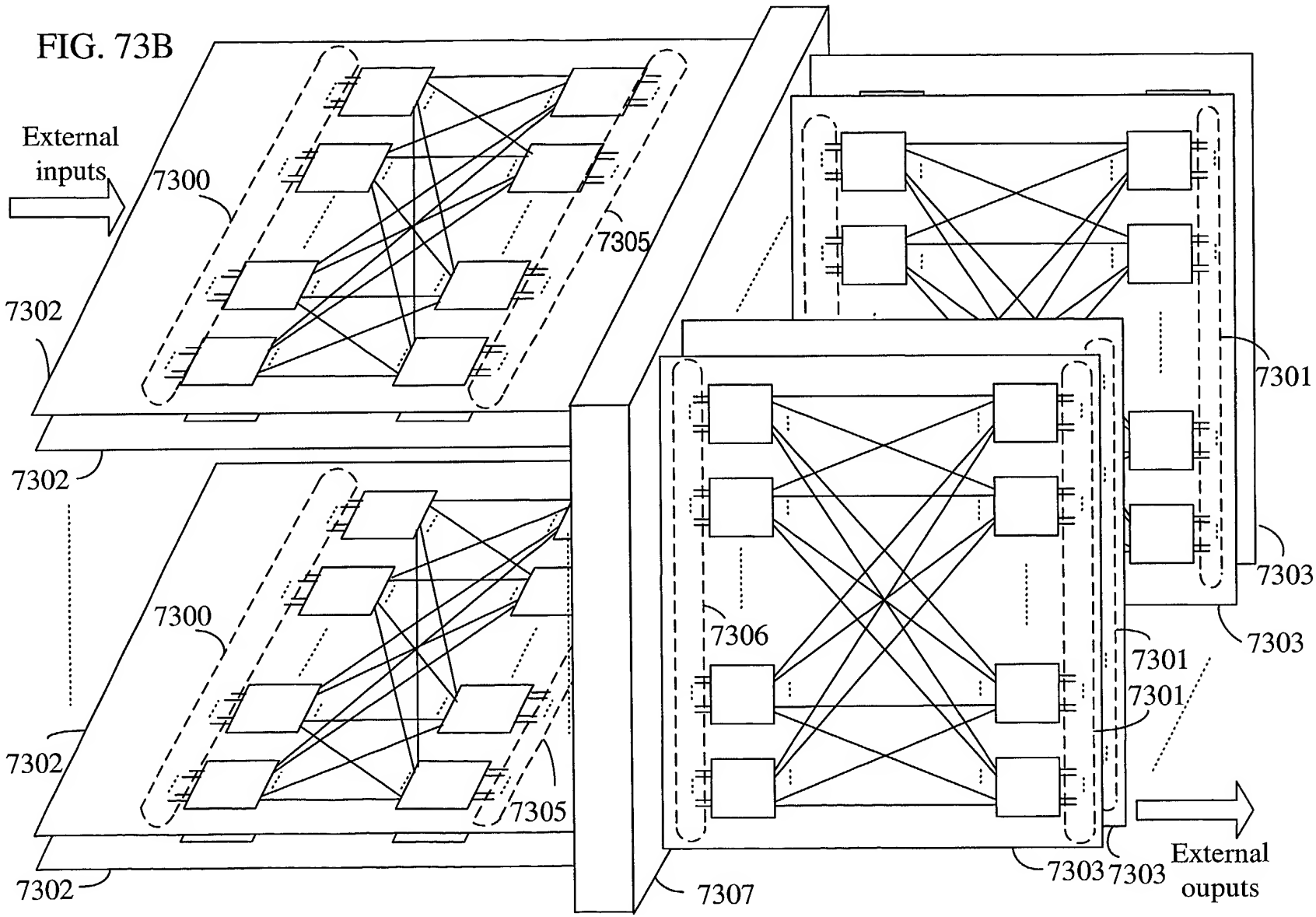

External inputs
7300
7305
7302
7304
7306
7301
7303
External ouputs

FIG. 73A

FIG. 73B


External inputs
7300
7305
7302
7302
7300
7305
7302
7307
7306
7301
7303
7301
7303
7301
7303
7303
External ouputs

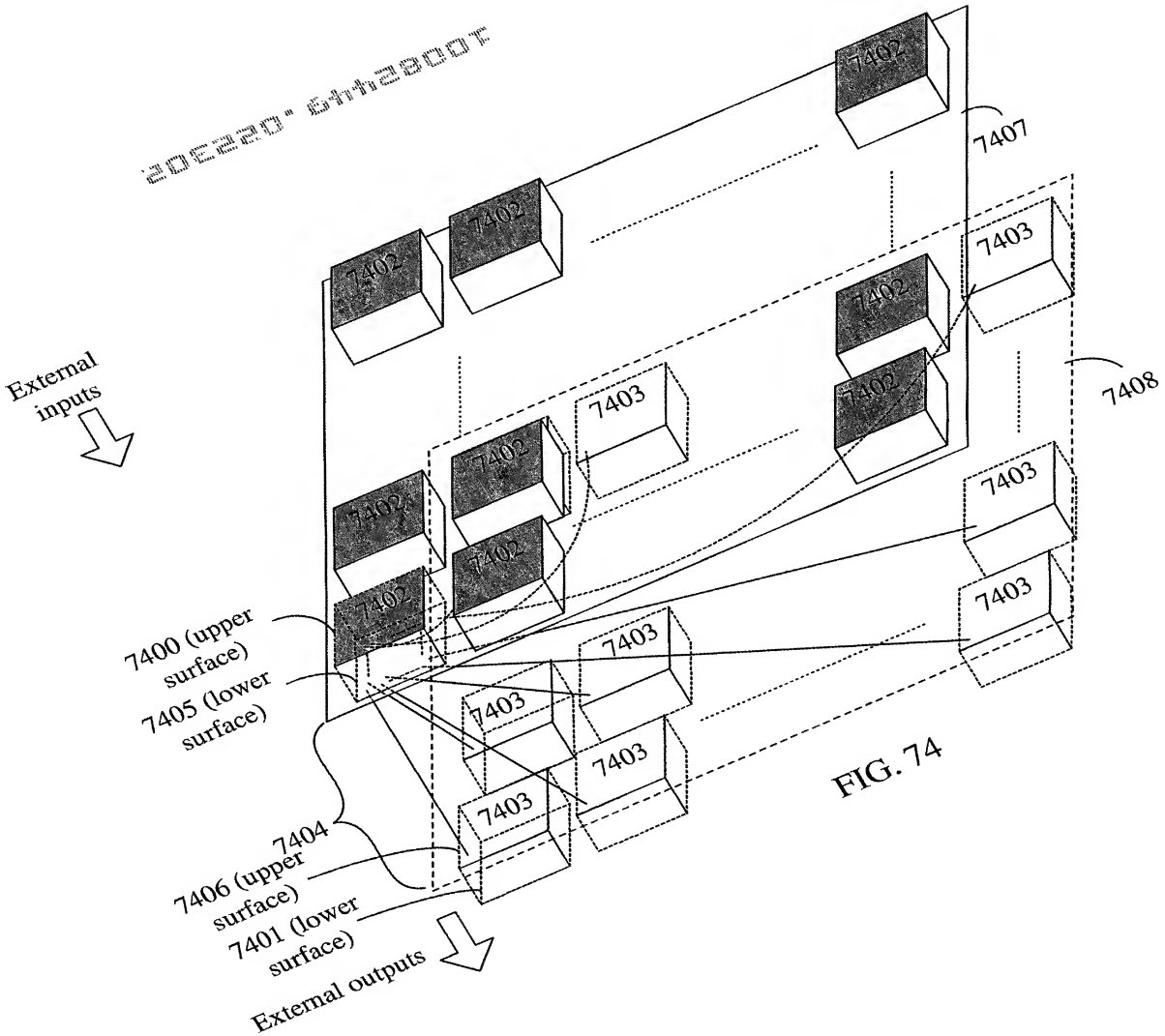

7402
7407
7403
7408
External inputs
7400 (upper surface)
7405 (lower surface)
7404
7406 (upper surface)
7401 (lower surface)
External outputs

FIG. 74

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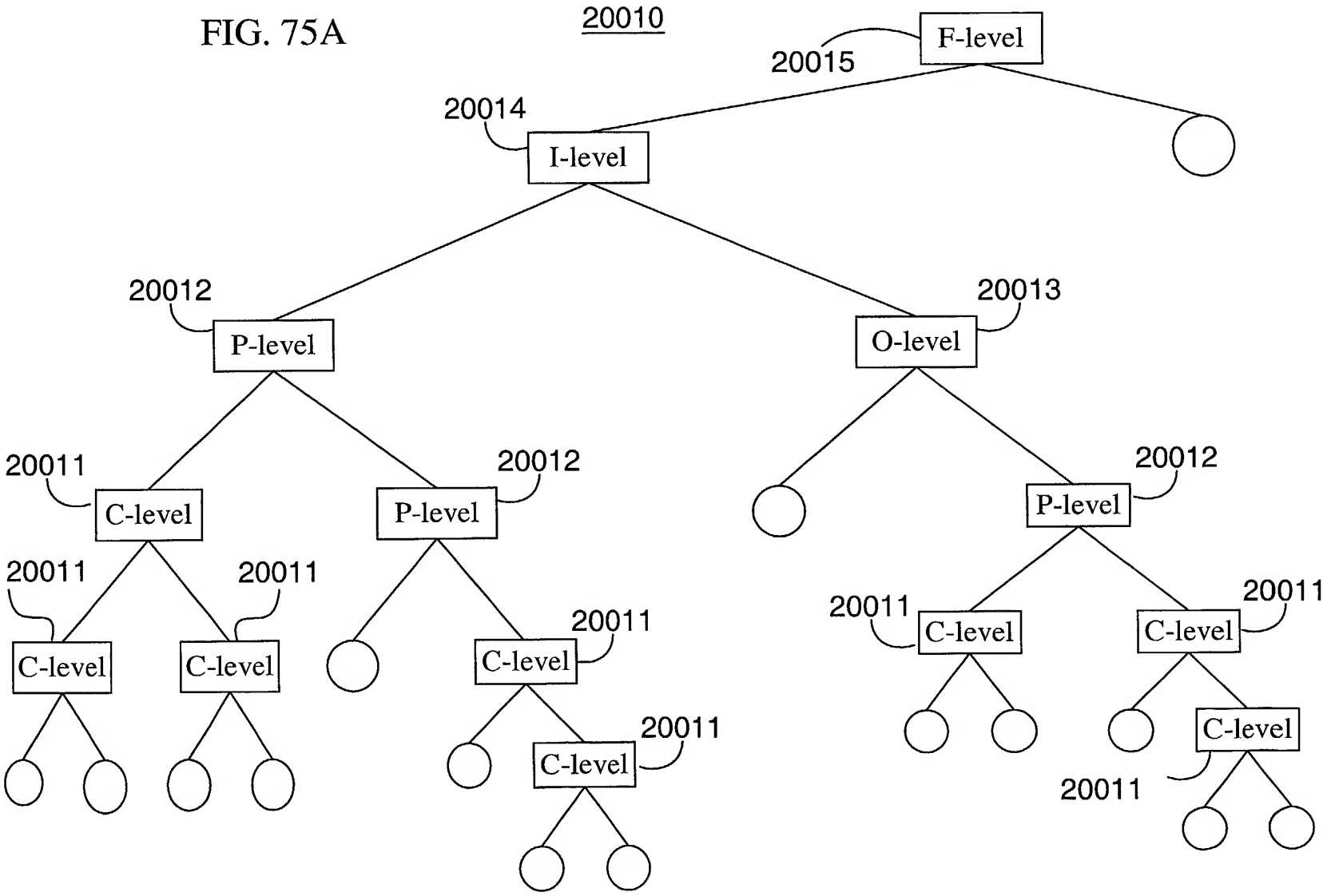
FIG. 75A



20220° 6th2807

FIG. 75B

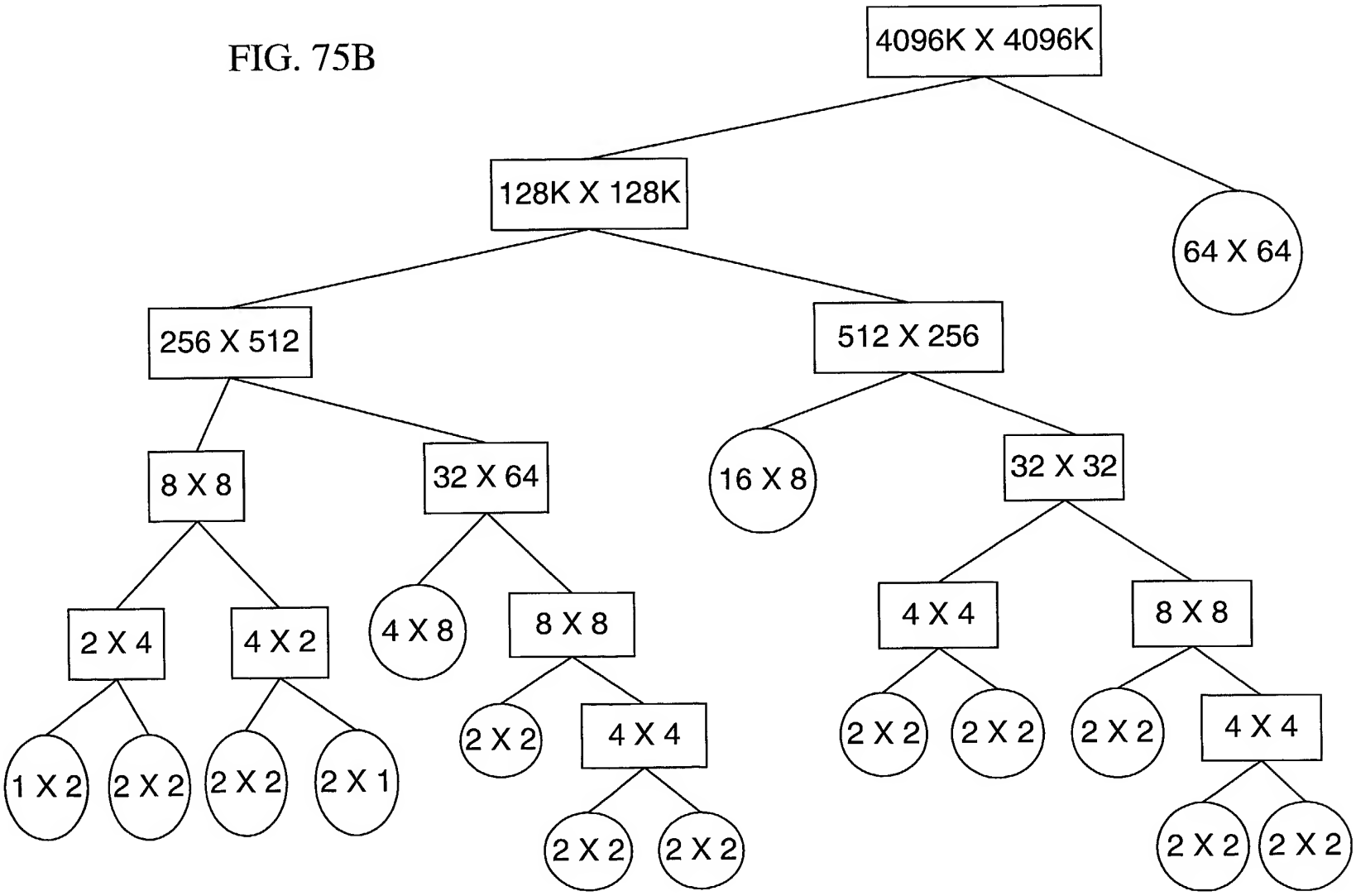
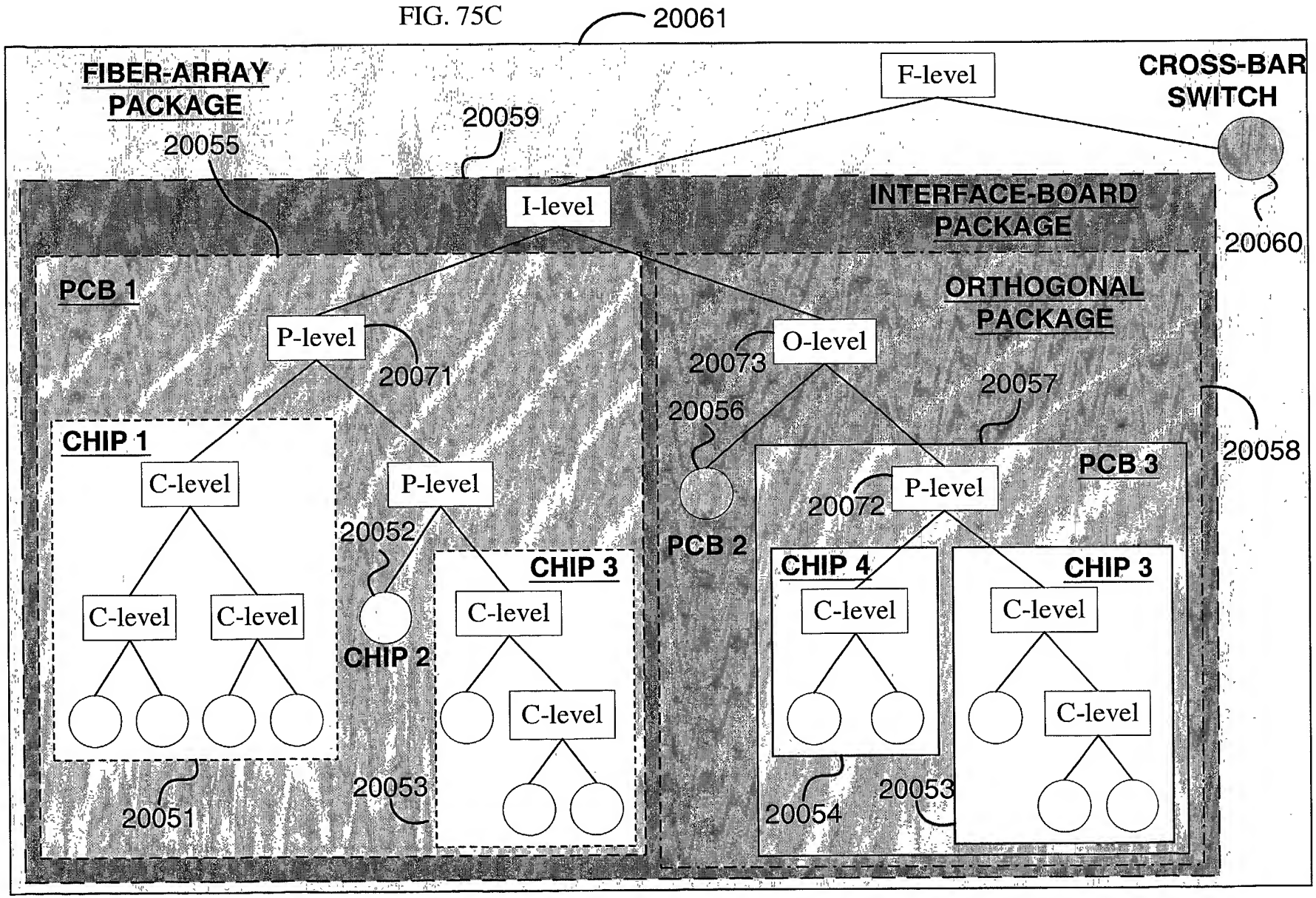


FIG. 75C


20061
FIBER-ARRAY PACKAGE
20055
20059
F-level
CROSS-BAR SWITCH
20060
I-level
INTERFACE-BOARD PACKAGE
PCB 1
P-level
20071
ORTHOGONAL PACKAGE
O-level
20073
20057
20056
20058
CHIP 1
C-level
P-level
PCB 3
20072
P-level
20052
PCB 2
CHIP 4
CHIP 3
C-level
C-level
C-level
C-level
CHIP 2
CHIP 3
C-level
C-level
C-level
20053
20053
20051
20054

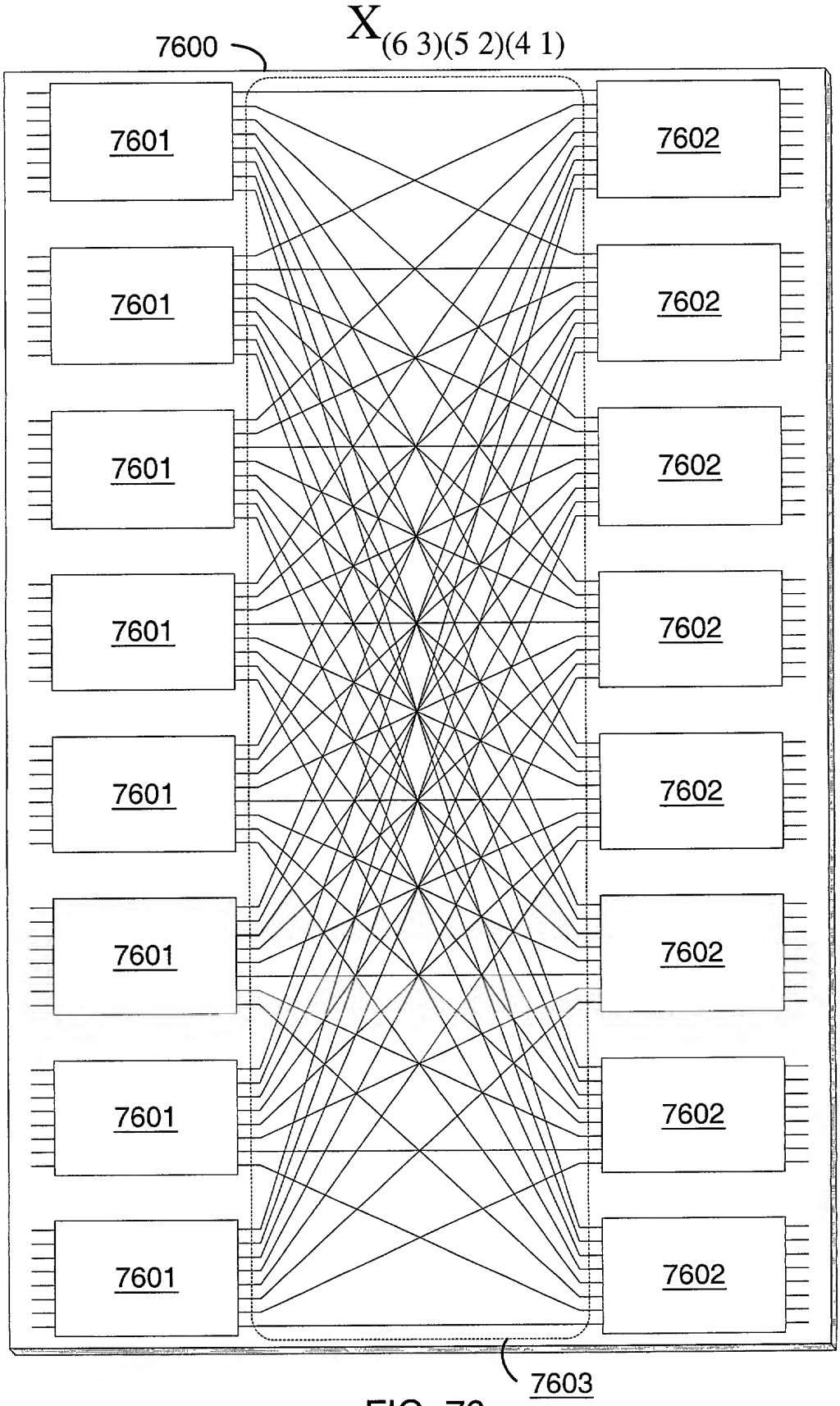


FIG. 76

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7700 $X_{(4\ 2)(3\ 1)}$

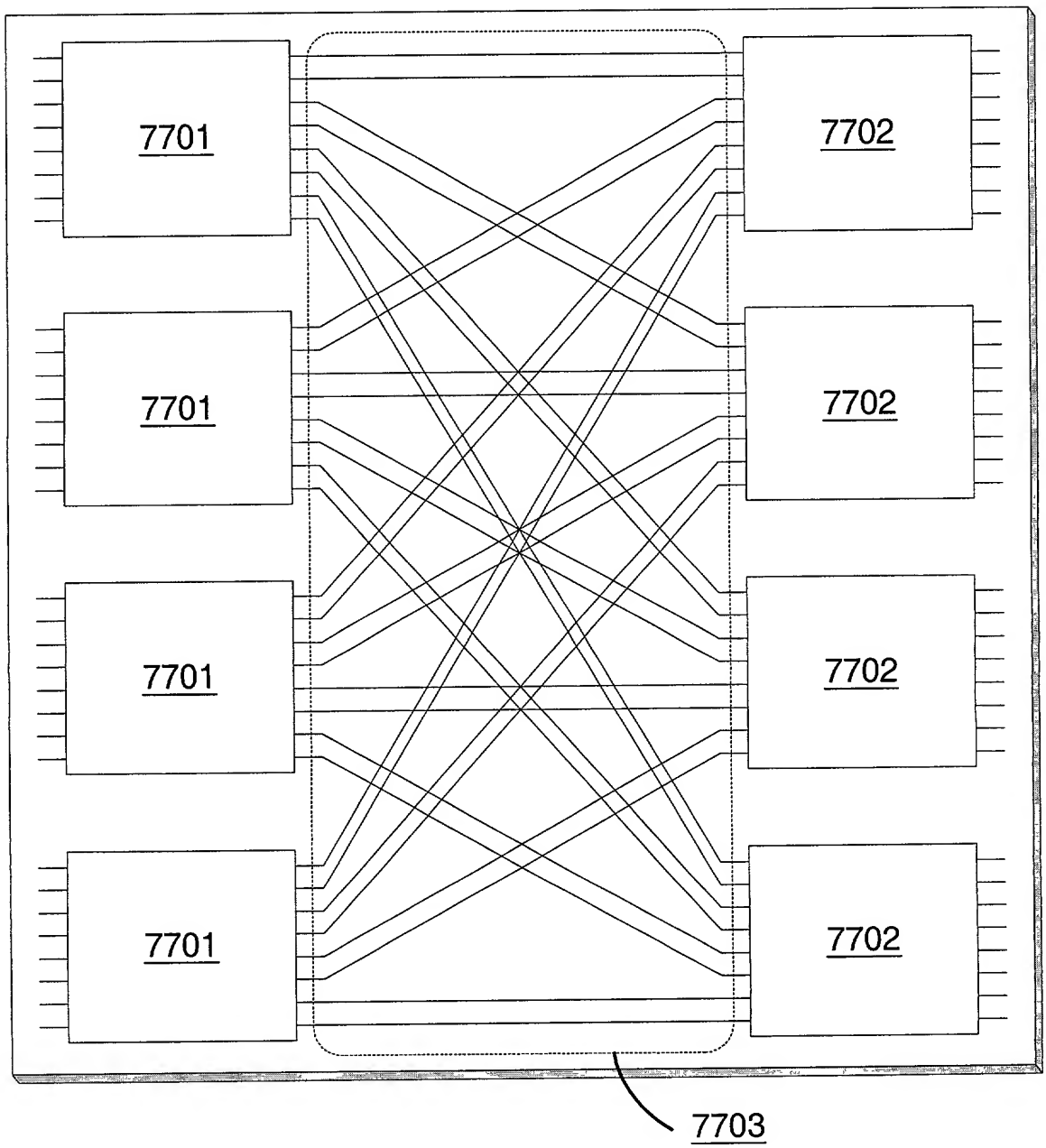

FIG. 77A

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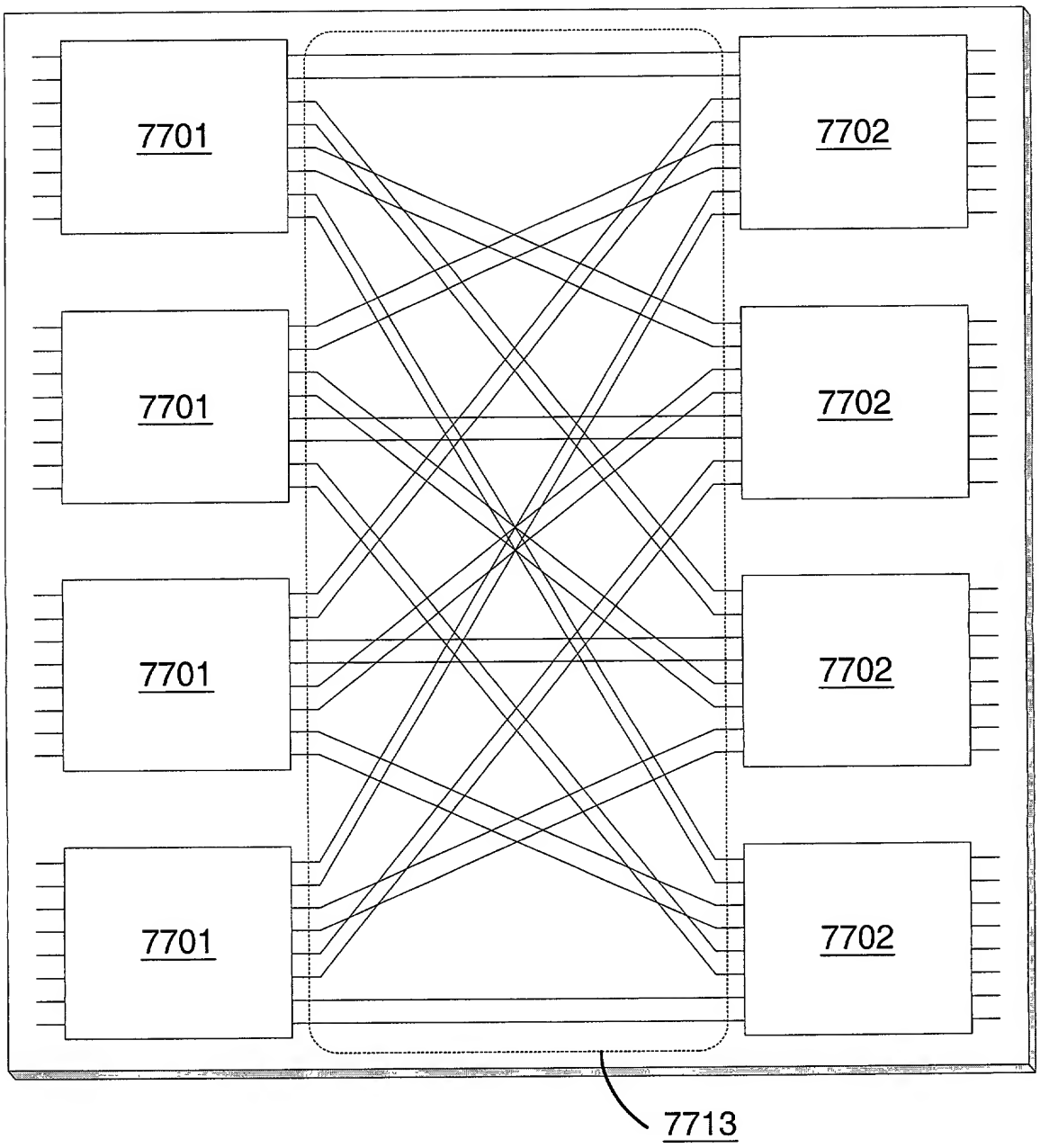

FIG. 77B

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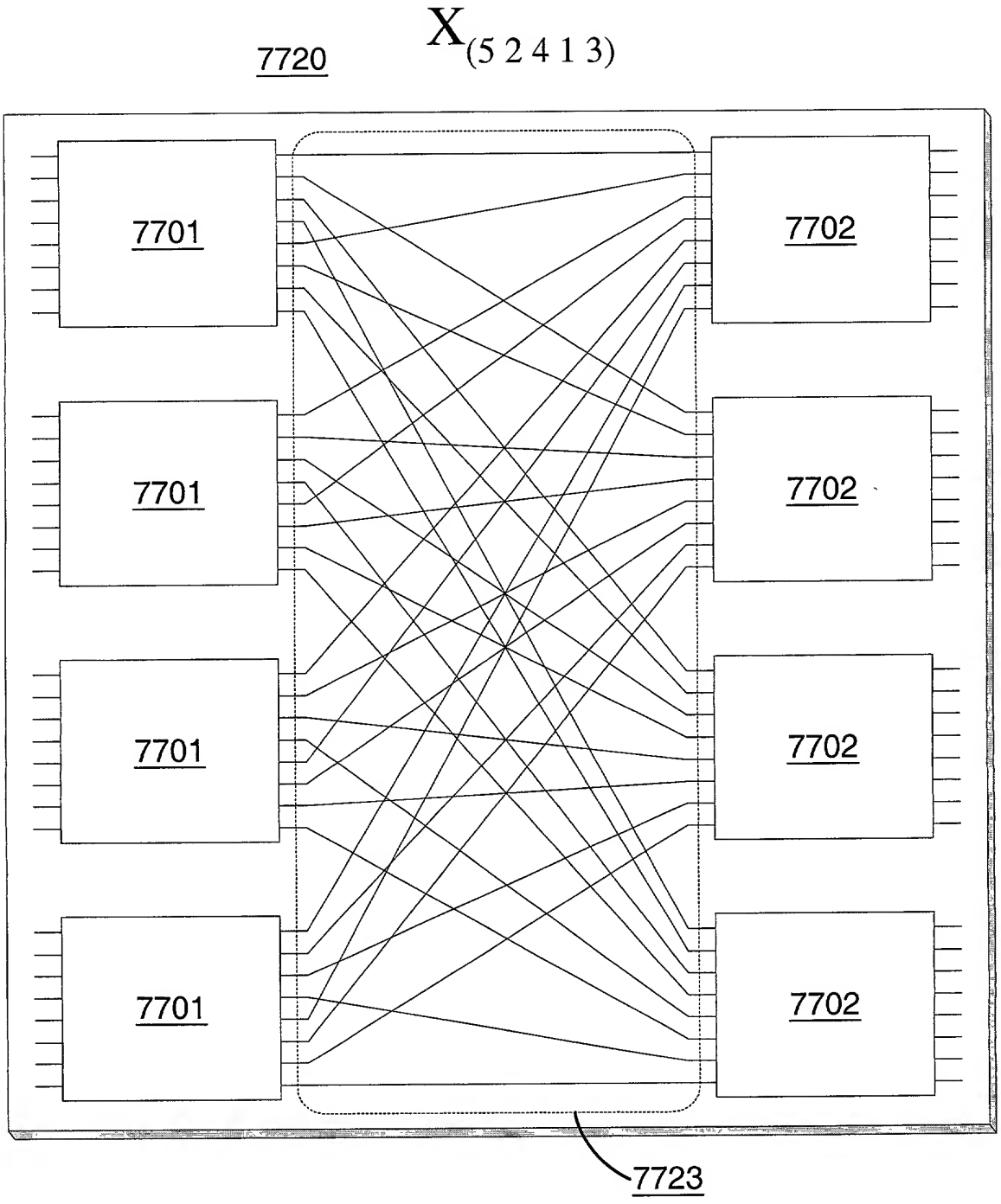

FIG. 77C

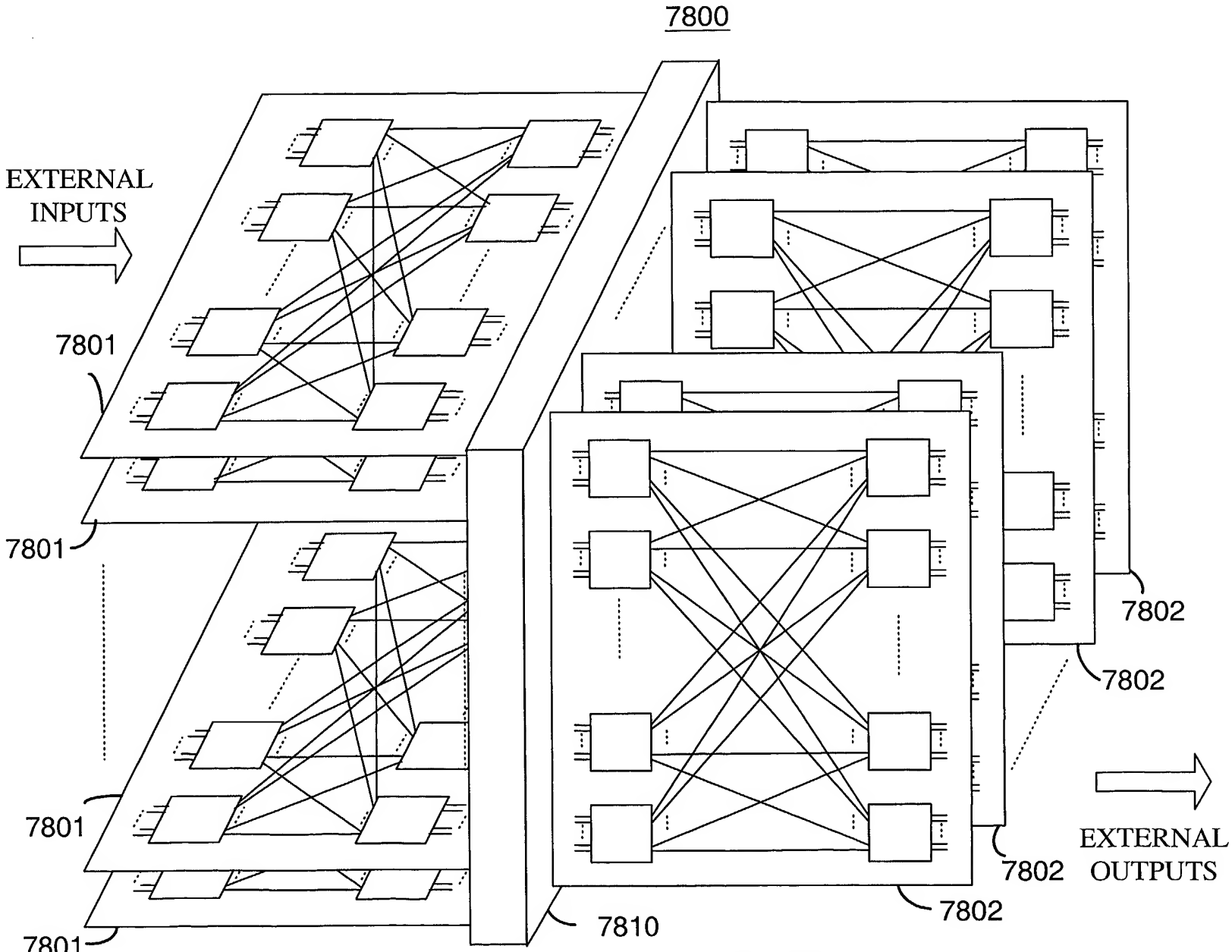
7800
EXTERNAL INPUTS
7801
7801
7801
7801
7802
7802
7802
7802
7810
EXTERNAL OUTPUTS

FIG. 78

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7900

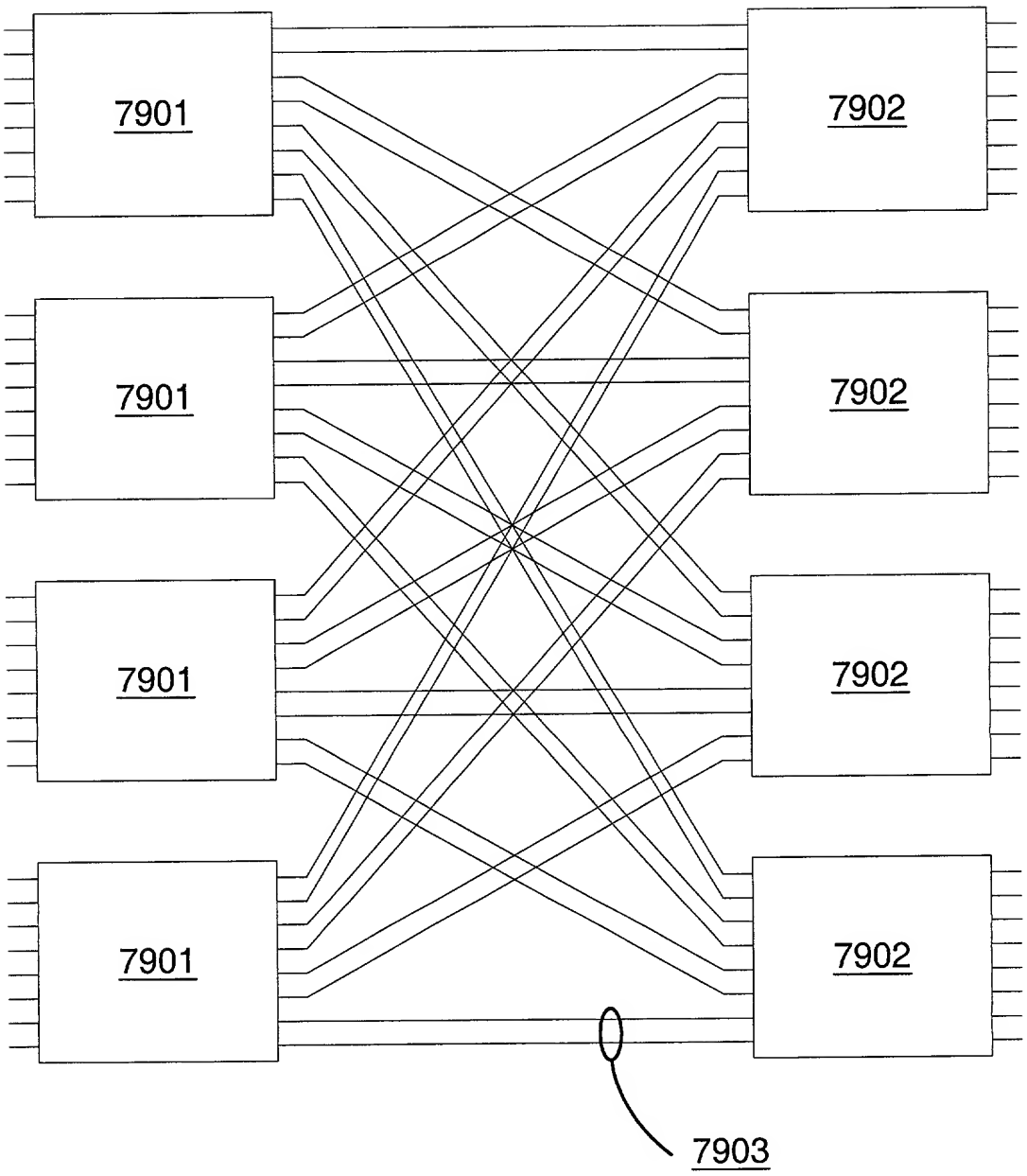

FIG. 79A

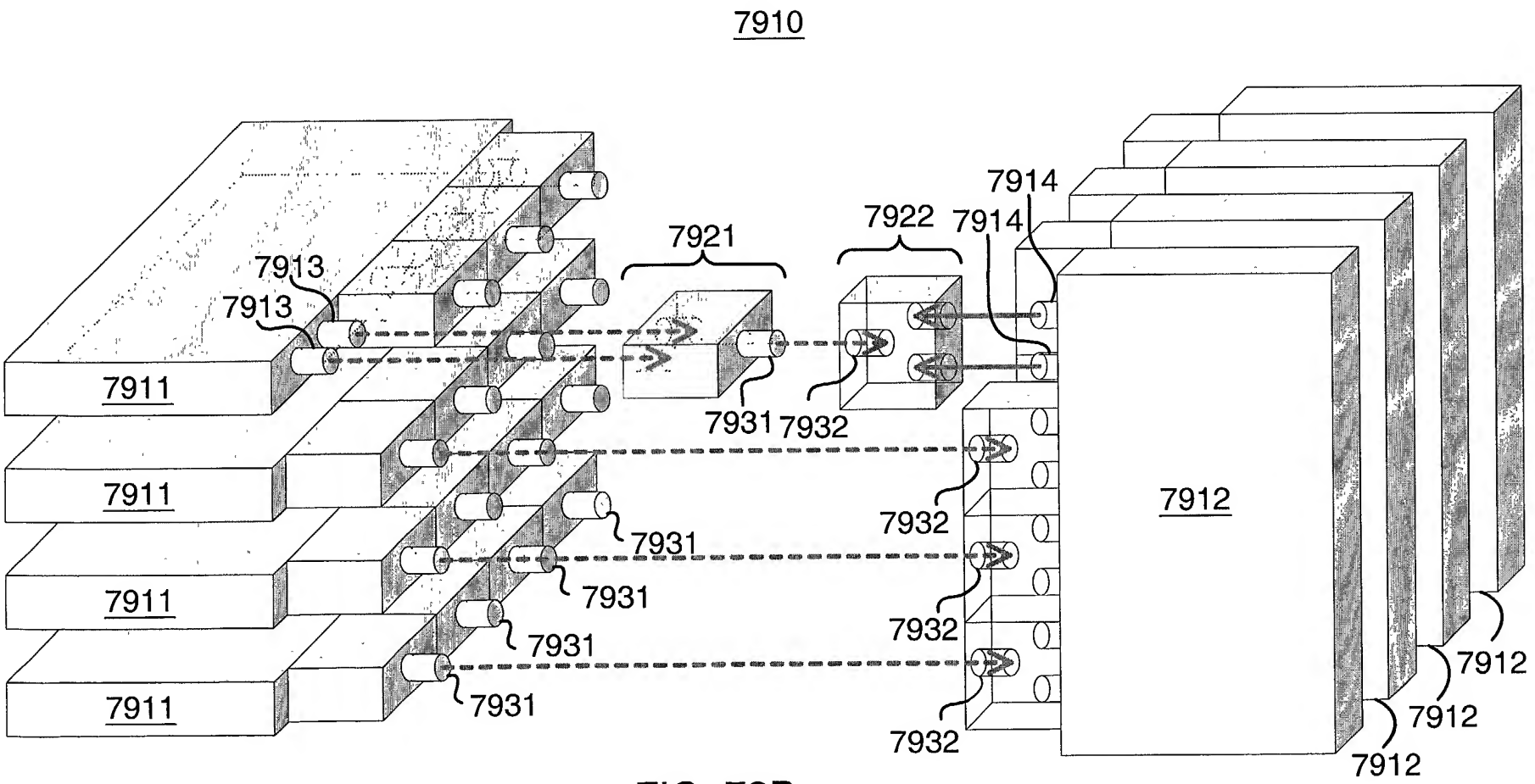
7910
7911
7911
7911
7911
7913
7913
7921
7922
7914
7914
7931
7931
7931
7931
7932
7932
7932
7932
7912
7912
7912
7912

FIG. 79B
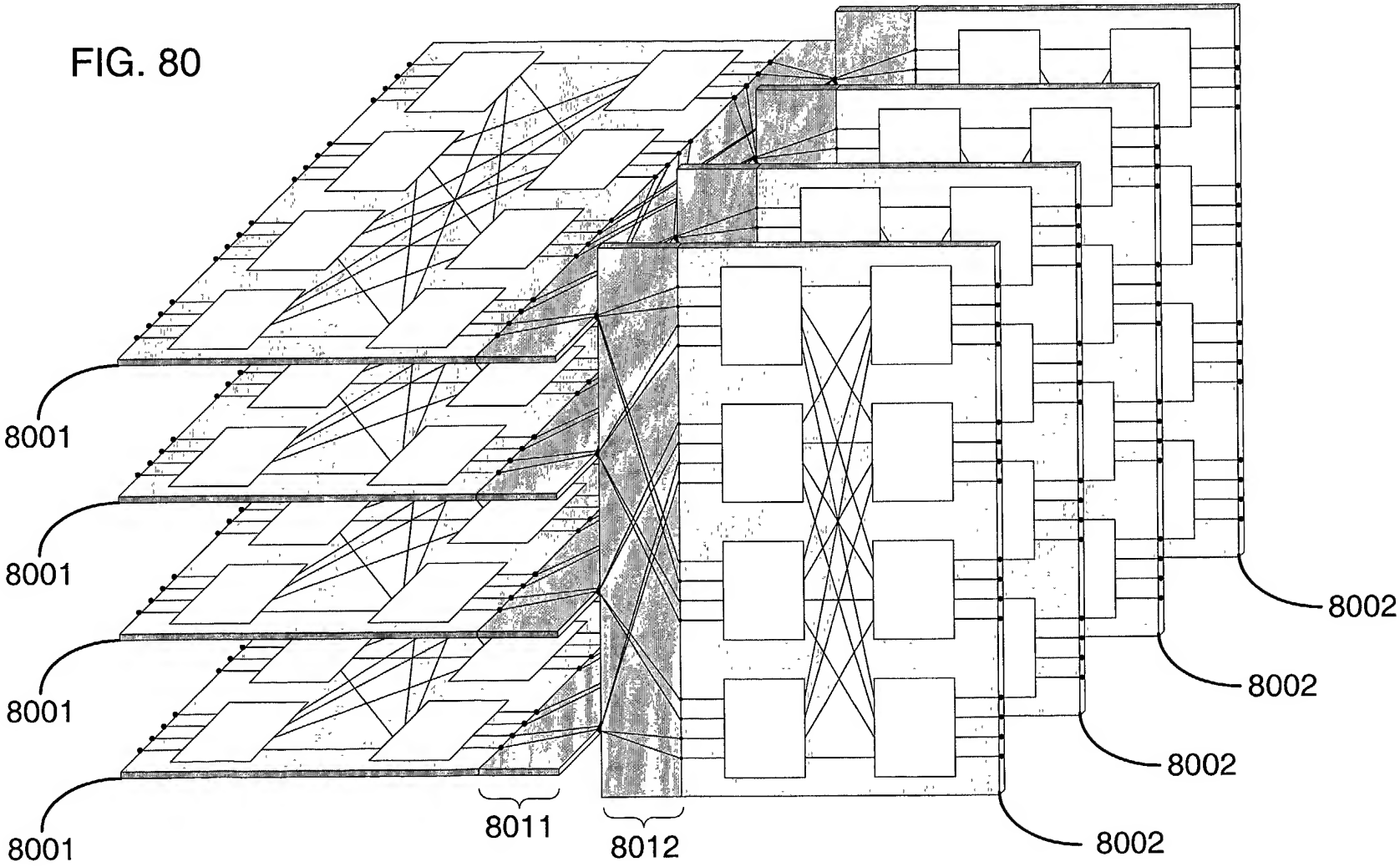
FIG. 80